# NSD12409-Q1

# 2CH, 90mΩ, 40V, Fully Protected Automotive Low-side Switch

Datasheet (EN) 1.2

## Product Overview

NSD12409-Q1 is a 90mΩ 2 channel low-side switch with 48V clamp voltage for automotive applications. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnose function is built to indicate any faults when thermal shutdown through an open-drain status output pin. This device operates in ambient temperatures from –40°C to 125°C.

## Key Features

- AEC-Q100 (Grade 1) qualified for auto-motive application
- Drain current limitation: 8A
- 48V overvoltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block
  - Thermal shutdown diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection
- RoHS & REACH Compliance

## Applications

- Automotive Relays
- Valves
- Solenoid drivers
- Lighting

## Device Information

| Part Number | Package | Body Size |
|---|---|---|
| NSD12409-Q1SPR | SO-8 | 4.9mm X 3.9mm |

## Typical Application

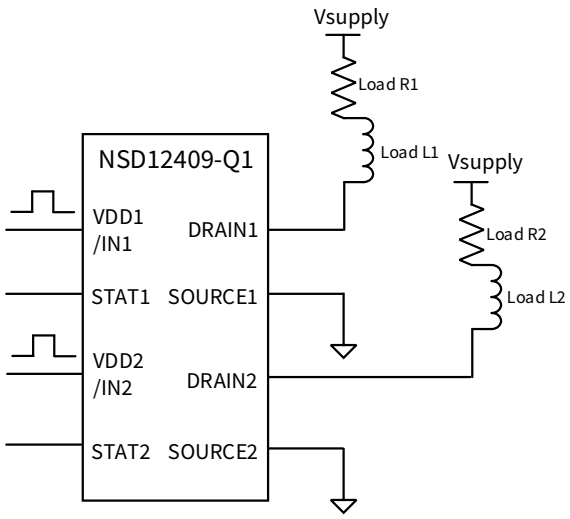



Figure 0.1 NSD12409-Q1 Typical Application

# INDEX

# 1. Pin Configuration and Functions

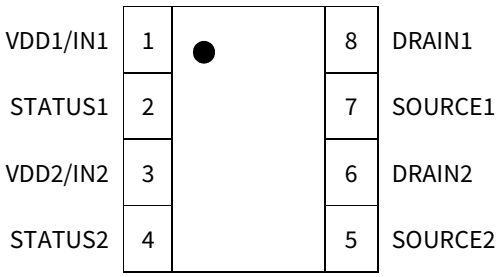



Figure 1.1 NSD12409-Q1 Pinout

Table 1.1 SO-8 Pin Configuration and Description

| PIN NO. | SYMBOL | FUNCTION |
|---|---|---|
| 1,3 | VDD1,2/IN1,2 | Voltage controlled input pin with hysteresis, CMOS compatible. They control output switch state |
| 2,4 | STATUS1,2 | Open drain digital diagnostic pin |
| 8,6 | DRAIN1,2 | PowerMOS drain |
| 7,5 | SOURCE1,2 | PowerMOS source and ground reference for the control section |

# 2. Block diagram

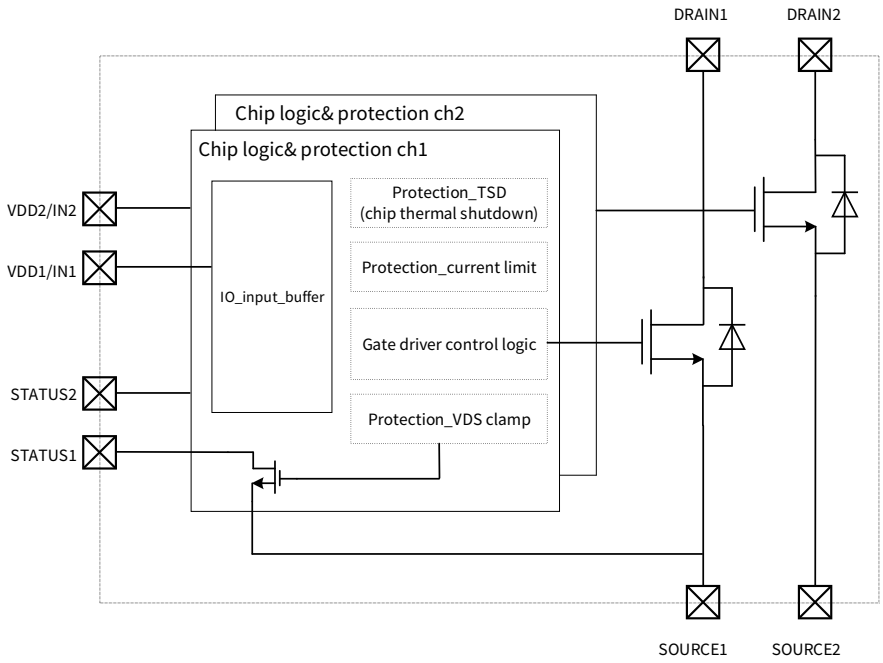



Figure 2.1 NSD12409-Q1 Block diagram

## 3. Absolute Maximum Ratings

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | | | Internally clamped | V |
| DC Drain Current | $I_D$ | | | Thermal limited | A |
| VDD/INPUT Pin Current | $I_{IN}$ | -1 | | 10 | mA |
| STATUS Pin Current | $I_{STAT}$ | -1 | | 10 | mA |
| Junction Temperature | $T_J$ | -40 | | 150 | °C |
| Storage Temperature | $T_{stg}$ | -55 | | 150 | °C |
| Single pulse avalanche energy (L = 3mH; $T_J$ = 150 °C; $R_L$ = 0; $I_{OUT}$ = $I_{lim}$) | $E_{AS}$ | | | 50 | mJ |

## 4. ESD ratings

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| V(ESD) Electrostatic discharge | Human-body model, per AEC-Q100-002-RevD， $V_{ESD-HBM}$ | ±4000 | V |
| | Charged-device model, per AEC-Q100-011-RevB， $V_{ESD-CDM}$ | ±750 | V |

## 5. Thermal Information

| Parameters | Symbol | SO-8 | Unit |
|---|---|---|---|
| Junction-to-ambient Thermal Resistance | $\theta_{JA}$ | 75.4 | °C/W |
| Junction-to-top characterization parameter | $\psi_{JT}$ | 4 | °C/W |
| Junction-to-case (top) thermal resistance | $\theta_{JC(top)}$ | 23.8 | °C/W |

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layers board.

# 6. Specifications

## 6.1. Electrical Characteristics

(VDD = VIN= 4.5 V to 5.5 V, $T_J$=-40°C to 150°C. Unless otherwise noted.)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| **Power MOSFET** | | | | | | |
| ON-state resistance | $R_{ON}$ | | 90 | | mΩ | $I_D$ = 1.6 A; $T_J$ = 25°C; $V_{DD}$ = $V_{IN}$ = 5 V |
| | | | | 180 | mΩ | $I_D$ = 1.6 A; $T_J$ = 150°C; $V_{DD}$ = $V_{IN}$ = 5 V |
| Drain-source clamp voltage | $V_{CLAMP}$ | 46 | 48 | 56 | V | $V_{IN}$ = 0V, $I_D$ = 1.6 A |
| Drain-source clamp threshold voltage | $V_{CLTH}$ | 40 | | | V | $V_{IN}$ = 0V, $I_D$ = 2 mA |
| OFF-state output current | $I_{DSS}$ | 0 | | 3 | μA | $V_{IN}$ = 0 V; $V_{DS}$ = 13 V; $T_J$ = 25°C |
| | | 0 | | 5 | μA | $V_{IN}$ = 0 V; $V_{DS}$ = 13 V; $T_J$ = 125°C |
| Body diode forward voltage | $V_{BD}$ | | 0.8 | | V | $I_D$ = 1.6 A; $V_{IN}$ = 0 V |
| **Input section** | | | | | | |
| Supply current from input pin | $I_{ISS}$ | | 25 | 65 | μA | ON-state; $V_{DD}$=$V_{IN}$ = 5 V; $V_{DS}$ = 0 V |
| Input clamp voltage | $V_{ICL}$ | 5.5 | | 8 | V | $I_{ICL}$ = 1 mA |
| | | | -0.7 | | | $I_{ICL}$ = -1 mA |
| Input threshold voltage | $V_{INTH}$ | 1 | | 3.5 | V | $V_{DS}$ = $V_{IN}$; $I_D$ = 1 mA |
| **Status indicator** | | | | | | |
| Status low output voltage | $V_{STAT}$ | | | 0.5 | V | $I_{STAT}$ = 1 mA |
| Status leakage current | $I_{LSTAT}$ | | | 10 | μA | $V_{STAT}$ = 5 V |
| Status pin input capacitance | $C_{STAT}$ | | | 100 | pF | $V_{STAT}$ = 5 V |
| Status clamp voltage | $V_{STCL}$ | 5.5 | | 8 | V | $I_{STAT}$ = 1 mA |
| | | | -0.7 | | | $I_{STAT}$ = - 1 mA |
| **Switching characteristics** | | | | | | |
| Turn-on delay time | $t_{d\,(ON)}$ | | 6 | | μs | $R_L$ = 8.2 Ω, $V_{CC}$ = 13V |
| Turn-off delay time | $t_{d\,(OFF)}$ | | 11 | | μs | $R_L$ = 8.2 Ω, $V_{CC}$ = 13V |
| Rise time | $t_r$ | | 5.7 | | μs | $R_L$ = 8.2 Ω, $V_{CC}$ = 13V |
| Fall time | $t_f$ | | 4.5 | | μs | $R_L$ = 8.2 Ω, $V_{CC}$ = 13V |
| Switching energy losses at turn-on | $W_{ON}$ | | 17 | | μJ | $R_L$ = 8.2 Ω, $V_{CC}$ = 13V |

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Switching energy losses at turn-off | $W_{OFF}$ | | 38 | | μJ | $R_L$ = 8.2 Ω, $V_{CC}$ = 13V |
| **Protection and diagnostics** | | | | | | |
| DC short-circuit current | $I_{lim}$ | 5.5 | 8 | 10.5 | A | $V_{DS}$ = 13 V, $V_{DD}$ = $V_{IN}$ = 5V |
| Shutdown temperature | $T_{TSD}$ | 150 | 175 | 200 | °C | |
| Reset temperature | $T_R$ | $T_{RS}$ + 1 | $T_{RS}$ + 5 | | °C | |
| Thermal reset of STATUS | $T_{RS}$ | 135 | | | °C | |
| Thermal hysteresis ($T_{TSD}$ - $T_R$) | $T_{HYST}$ | | 7 | | °C | |
| Dynamic temperature | $\Delta T_J$ | | 40 | | K | $T_J$ = -40°C, $V_{CC}$ = 13V |
| Dynamic temperature hysteresis | $\Delta T_{J\,(HYS)}$ | | 15 | | K | |

## 6.2. Typical Performance Characteristics

### 6.2.1. True table

| Conditions | Input | Drain | Status |
|---|---|---|---|
| Normal operation | L | H | H |
| | H | L | H |
| Current limitation | L | H | H |
| | H | X | H |
| Over-temperature limitation | L | H | H |
| | H | H | L |
| VDD under-voltage | L | H | X |
| | H | H | X |

### 6.2.2. Switching characteristics

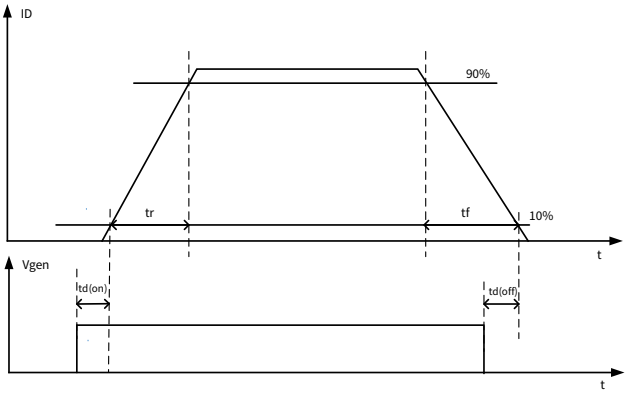



Figure 6.2.2 NSD12409-Q1 Switching Characteristics

# 7. Protections

## 7.1. Current Limitation

NSD12409-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to battery.

## 7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and another one on the controller is the coldest. The absolute temperature protection is to shut down the MOSFET when the hottest junction temperature exceeds the $T_{TSD}$, and the dynamic temperature protection is also to shut down the MOSFET when the temperature difference between the hottest and the coldest exceeds $\Delta T_J$.

# 8. Application information

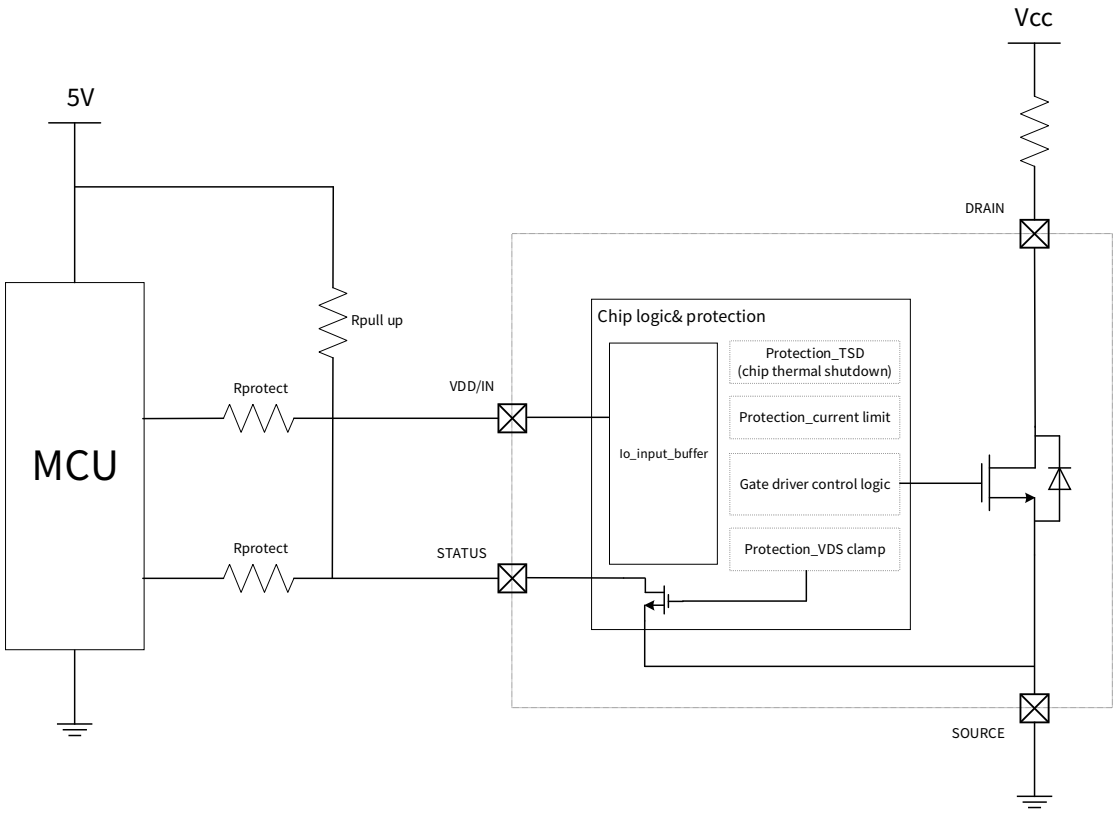



Figure 8.1 NSD12409-Q1SPR application schematic

## 8.1. MCU I/O protection

NSD12409 has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

$$\frac{0.7}{I_{latchup}} \le R_{prot} \le \frac{V_{MCU\_OUT} - V_{IH}}{I_{IHmax}}$$

Where $I_{latchup}$ is the MCU I/O latch up current, $V_{MCU\_OUT}$ is the output voltage of MCU I/O, $V_{IH}$ is the High-level input voltage of NSD12409, $I_{IH}$ is the High-level input current.

Let: $I_{latchup} \ge 20mA$; $V_{MCU\_OUT} \ge 4.5V$, so $35\Omega \le R_{prot} \le 15k\Omega$, the recommended value is $1k\Omega$.

## 8.2. The value of STATUS pulls up resistor

Because the STATUS pin is open drain output, a pull up resister is needed to fix the high voltage during normal operation. When the fault occurs, the voltage level of STATUS is pulled down by the internal MOSFET on. The value of pull up resistor can be calculated by the formula as shown below:

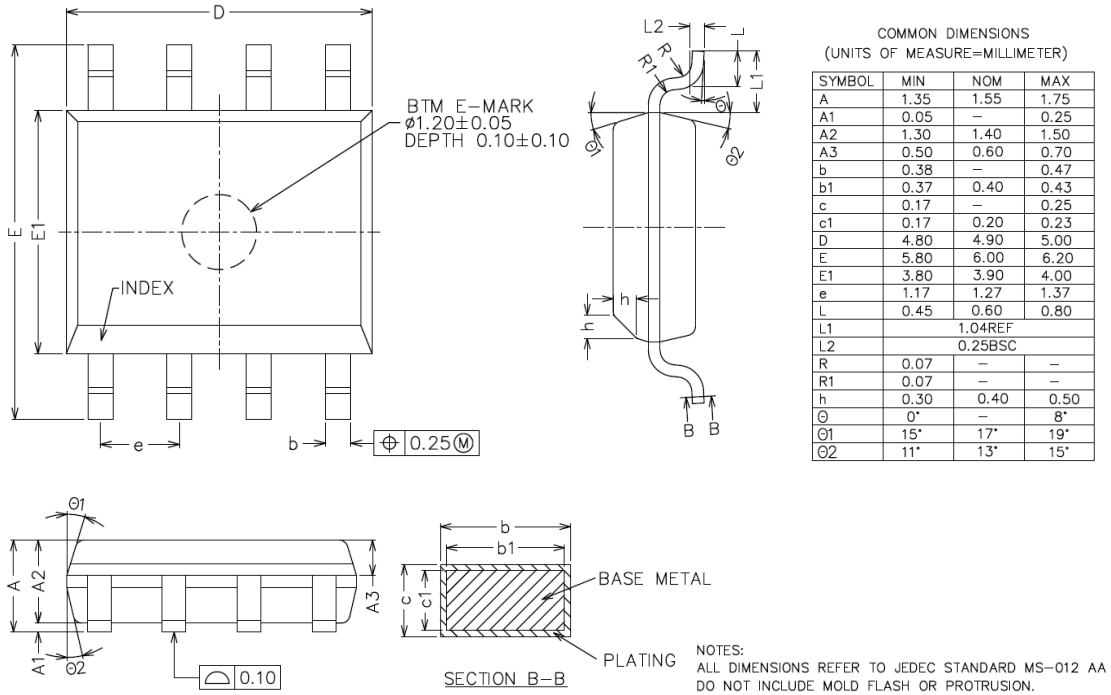
$$\left(\frac{V_{pull\text{-}up}}{V_{OL}} - 1\right) \cdot R_{on} < R_{pull\text{-}up} < \frac{V_{pull\text{-}up} - V_{OH}}{I_{leak}}$$

Where $V_{pullup}$ is the minimum of pull-up supply, $V_{OL}$ is the maximum of MCU logic low, $R_{on}$ is the on resistance of the MOSFET of STATUS pin, $V_{OH}$ is the minimum of MCU logic high, $I_{leak}$ is the maximum leakage current of STATUS pin.

Let: $V_{pullup} = 4.5V$; $R_{on} = V_{STAT}/I_{STAT} = 500\Omega$, $V_{OL} = 0.9V$; $V_{OH} = 2.1V$; $I_{leak} = 10uA$, so $2k\Omega \le R_{pullup} \le 240k\Omega$.

# 9. Package Information

## 9.1. SO-8 package information

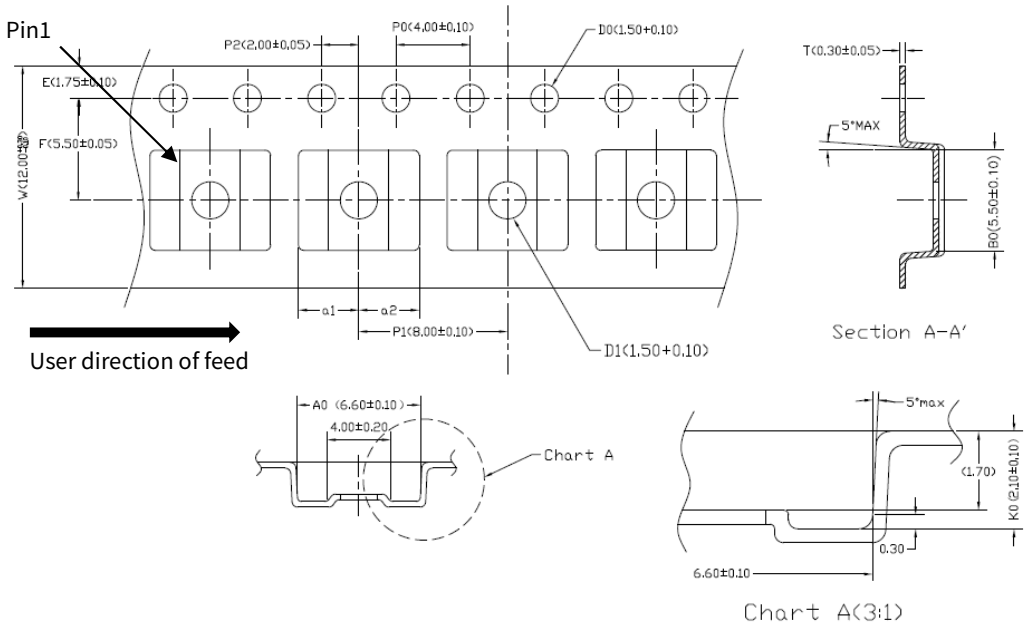


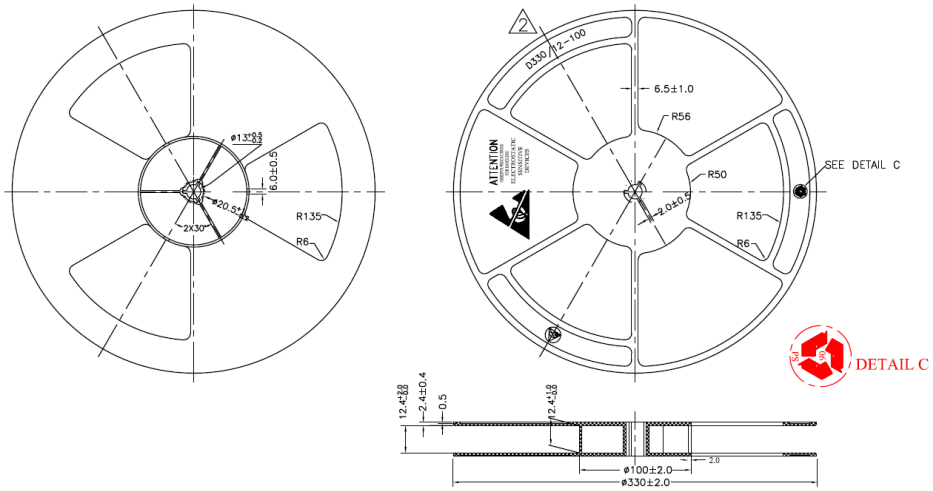

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.05 | – | 0.25 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.50 | 0.60 | 0.70 |
| b | 0.38 | – | 0.47 |
| b1 | 0.37 | 0.40 | 0.43 |
| c | 0.17 | – | 0.25 |
| c1 | 0.17 | 0.20 | 0.23 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.17 | 1.27 | 1.37 |
| L | 0.45 | 0.60 | 0.80 |
| L1 | 1.04REF | | |
| L2 | 0.25BSC | | |
| R | 0.07 | – | – |
| R1 | 0.07 | – | – |
| h | 0.30 | 0.40 | 0.50 |
| Θ | 0° | – | 8° |
| Θ1 | 15° | 17° | 19° |
| Θ2 | 11° | 13° | 15° |

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

## 9.2. SO-8 packaging information



# 10. Ordering Information

| Part Number | Package | MSL | SPQ |
|---|---|---|---|
| NSD12409-Q1SPR | SO-8 | 3 | 2500 |
| Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature. | | | |

# 11. Revision History

| Revision | Description | Date |
|---|---|---|
| 1.0 | Initial version | 2024/1/30 |
| 1.1 | Change the ESD writing format | 2024/4/18 |
| 1.2 | Update the titles of graphs and tables | 2024/5/8 |

# IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’ products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

**Suzhou NOVOSENSE Microelectronics Co., Ltd**