Application Note

NOVOSENSE

EMC Circuit of NSPGL1

AN-12-0044

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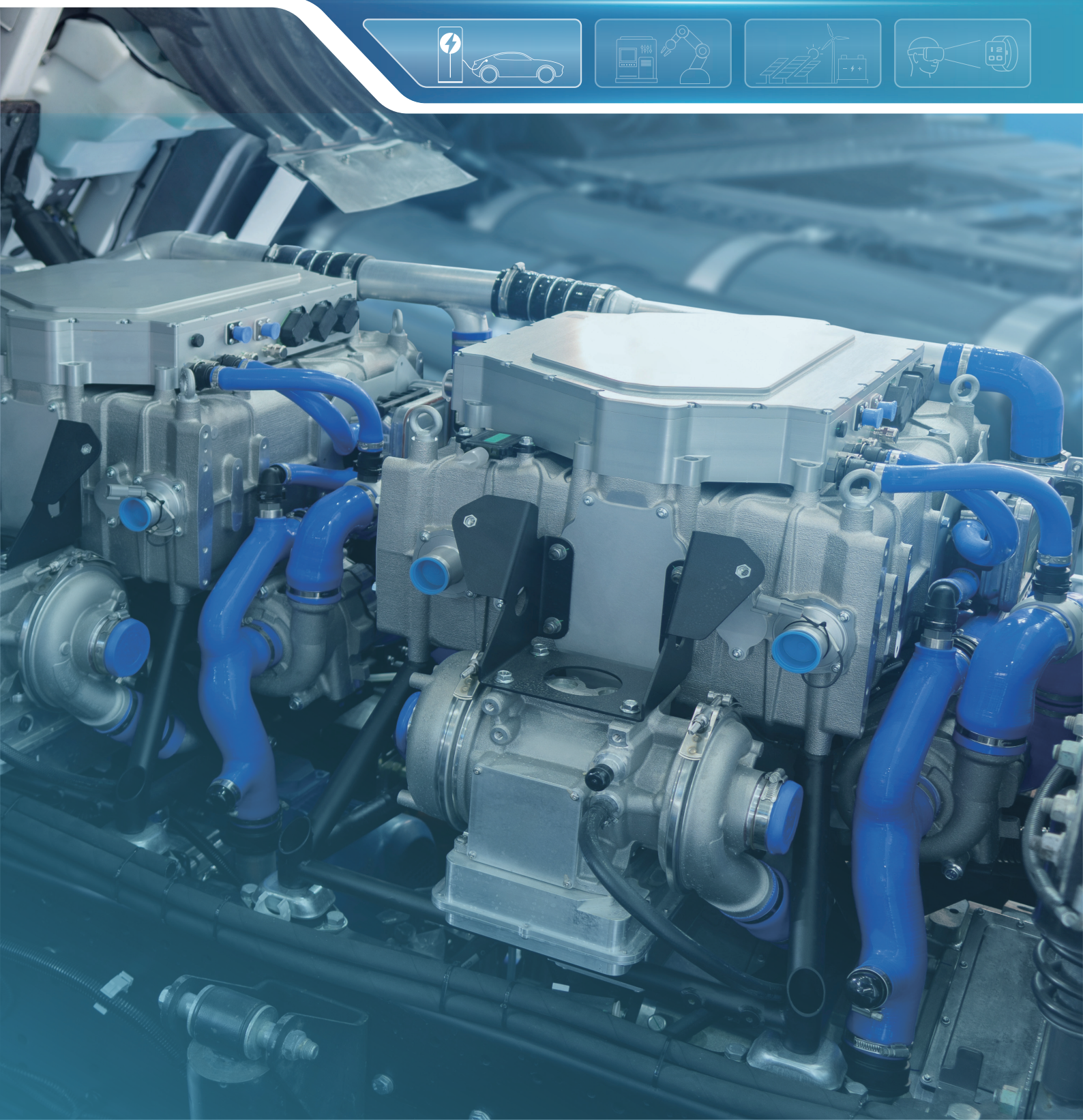

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ABSTRACT

This application note introduces an EMI & ESD enhanced application circuit of NSPGL1 and suggests some practical PCB layout guidelines to provide cost-effective protection against bulk current injection (BCI) and electrostatic discharge (ESD). According to the EMC requirement, the recommended circuit could be used as a reference in application and minor modification could be conducted based on the original circuit.

INDEX

1.Hardware

1.1.EMI & ESD Enhanced Edition

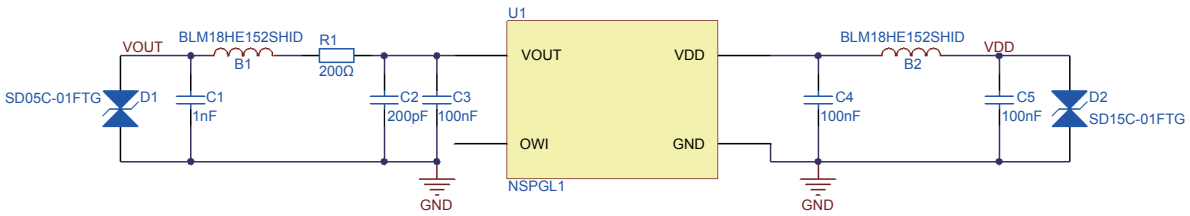

Figure 1.1 EMI & ESD enhanced application circuit

1.1.1.EMC Performance

Items	Standards	Type	Network	Parameter	Severity
ESD(Power off)	ISO 10605:2008	Contact discharge	150pF 330Ω	±20KV	Class C
		Air discharge		±20KV	Class C

Items	Standards	Type	Parameter	Test Level	Severity
BCI	ISO 11452-4:2020	CBCI	0.1MHz-400MHz	200mA	Class A
		DBCI		100mA	Class C

Items	Standards	Pulse Type	Severity
Transient Conducted Immunity on Other Lines(CCC)	ISO 7637-3:2016	Fast 3a, Fast 3b	Class A

Items	Standards	Pulse Type	Severity
Transient Conducted Immunity on Other Lines(ICC)	ISO 7637-3:2016	Slow +, Slow -	Class A

Items	Standards	Frequency Parameter	Test Level	Severity
RI(ALSE Method)	ISO 11452-2:2019	80MHz-2000MHz	100V/m	Class A

Items	Standards	Frequency Parameter	Severity
RE(Radiated Emission)	CISPR 25:2008	0.15MHz-2500MHz	Class 5

Items	Standards	Frequency Parameter	Severity
CE(Current method)	CISPR 25:2008	0.15MHz-108MHz	Class 5

Items	Standards	Frequency Parameter	Severity
CE(Voltage method)	CISPR 25:2008	0.15MHz-108MHz	Class 5

1.1.2.Summary of Test Result

Suzhou Neotest Inspection and Testing Co., Ltd.
Report No.: NEO-EMC20240624002-EN
Page: 7 of 109

6. Summary of Test Result

Chapter No.	Test Items	Mode	Page	20240624002-1	20240624002-2	20240624002-3	Remark
11.1	ESD (DUT Unpowered)	Mode2	13	Pass	Pass	N/A	N/A
11.2	BCI	Mode1	16	Pass	Pass	N/A	N/A
11.3	RE	Mode1	22	Pass	Pass	N/A	N/A
11.4	CEC	Mode1	61	Pass	Pass	N/A	N/A
11.5	CEV	Mode1	77	Pass	Pass	N/A	N/A
11.6	RI	Mode1	93	Pass	Pass	N/A	N/A
11.7	CCC	Mode1	101	N/A	Pass	Pass	N/A
11.8	ICC	Mode1	106	N/A	Pass	Pass	N/A

Please contact NOVOSENSE for the detailed EMC test report of NSPGL1.

2.BOM

Comment	Designator	Footprint	Value	Type	Supplier
TVS	D1	SOD-323	—	SD15C-01FTG	Littelfuse
TVS	D2	SOD-323	—	SD05C-01FTG	Littelfuse
Bead	B1, B2	0603	—	BLM18HE152SH1D	muRata
Cap	C1	0402	1nF	CL05B102KB5VPNC	SAMSUNG
Cap	C2	0603	200pF	CL10B201KB8NNNC	SAMSUNG
Cap	C3, C4	0603	100nF	CL10B104KB8NNNC	SAMSUNG
Cap	C5	0402	100nF	CL05E104KB5VPNC	SAMSUNG
Resistor	R1	0603	200Ω	0603WAF2000T5E	UNI-ROYAL
NSPGL1	U1	LGA	—	NSPGL1L007RRA1	NOVOSENSE

3.Layout

The TVS protects the VDDHV and OUT pins from damage caused by transient high-voltage pulses. If the applied EMC environment is harsh, the TVS with higher power can be applied at the expense of a larger package size. On the PCB layout, it is necessary to place the two TVSs as close as possible to the connector.

The C4 capacitor filters out power-supply noises and keeps the power-supply stable. This capacitor should be placed as close as possible to the U1 VDD pins. Similarly, the C1 capacitor filters out noises from the signal line and keeps the output signal stable, which should be placed as close as possible to the output connector.

The beads suppress the noises from the power & signal lines during BCI test, which should be placed as close as possible to the connectors, directly connected to the power & signal lines.

Figure 3.1 demonstrates a PCB layout example of EMI & ESD enhanced application circuit for NSPGL1.

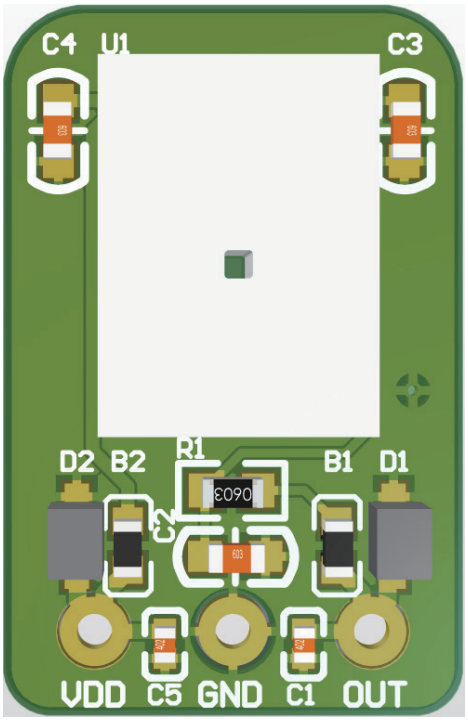

Figure 3.1 EMI & ESD enhanced application circuit PCB layout

Attention: All components should be placed at least 2mm away from the NSPGL1 for underfill process.

4.Function Performance Status Classification

Class	Description
Class A	The DUT can perform all its pre-designed functions during and after the interference is applied. The tolerances caused by the disturbance are within the design error range of the DUT.
Class B	During interference, the device under test can perform all its pre-designed functions; however, one or more indicators exceed the specified deviation. All functions automatically return to the normal working range after stopping the interference.

Class	Description
Class C	During interference, the DUT does not perform one or more of its pre-designed functions, which affects the normal operation of the basic functions of the entire system, but it can automatically return to normal operation after stopping the application of interference.
Class D	The DUT does not perform one or more of its pre-designed functions during the application of interference. It will not automatically return to its normal operating state until the application of interference is stopped and a simple "operation or use" reset action is performed.
Class E	During and after the interference is applied, the device under test does not perform one or more of its pre-designed functions, and if it does not repair or replace the device or system, it cannot resume its normal operation.

5.Revision History

Revision	Description	Author	Date
1.0	Initial version	Qiuliang Shi	2023/08/14
1.1	Add the result of DBCI.	Qiuliang Shi	2025/09/03

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