NCA1051A-Q1

High-speed CAN Transceiver

Datasheet (EN) 1.2

Product Overview

The NCA1051A-Q1 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The NCA1051A-Q1 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The NCA1051A-Q1 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- Ideal passive behavior to the CAN bus when the supply voltage is off
- I/O voltage range supports 3.3V and 5V MCU
- Power supply voltage
- V_{IO}: 2.8V to 5.5V
- V_{CC}: 4.5V to 5.5V
- Bus fault protection of -58V to +58V
- Bus common-mode voltage of -30V to +30V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Data rate: up to 5Mbps
- Low loop delay: <250ns
- Operation temperature: -40℃ to +125℃
- AEC-Q100 qualified for automotive, Grade 1
- RoHS & REACH compliant

Applications

- CAN bus standards such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783 and CANaerospace
- Highly loaded CAN networks down to 10 kbps networks
- Automotive gateway
- Body control modules
- Advanced Driver Assistance Systems (ADAS)
- Infotainment system

Device Information

Part Number	*Package*	*Body Size*
NCA1051A-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1051A-Q1DNR	DFN8	3.00mm × 3.00mm
NCA1051N-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1051N-Q1DNR	DFN8	3.00mm × 3.00mm

Functional Block Diagrams

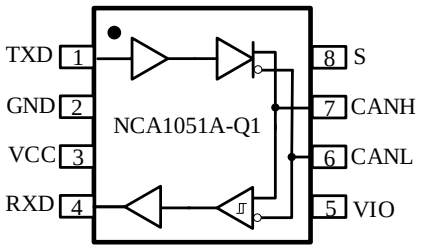


Figure 1. NCA1051A-Q1 Block Diagram

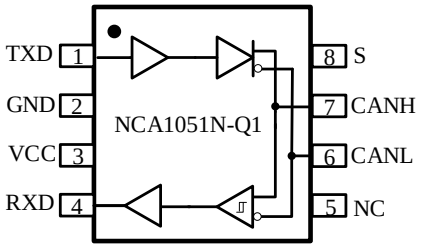


Figure 2. NCA1051N-Q1 Block Diagram

Index

1. Pin Configuration and Functions

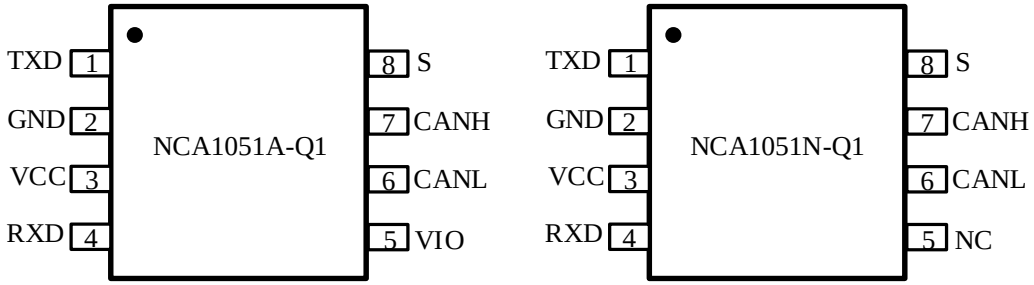


Figure 1-1 NCA1051A-Q1, NCA1051N-Q1 Package

Table 1-1 NCA1051A/N-Q1 Pin Configuration and Description

NCA1051A-Q1 PIN NO.	*NCA1051N-Q1 PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	2	GND	Ground
3	3	VCC	Power Supply
4	4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	\	VIO	Logic I/O supply voltage
\	5	NC	Not connected
6	6	CANL	Low-level CAN bus line
7	7	CANH	High-level CAN bus line
8	8	S	S (silent mode) select pin (active high)

2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1] [2].

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VCC, VIO	-0.3		7	V	
Logic I/O Voltage	TXD, RXD, S	-0.3		7	V	
Maximum bus Pin Voltage	V_{CANH}, V_{CANL}	-58		58	V	
Voltage between pin CANH and pin CANL	V_{CANH} - V_{CANL}	-58		58	V	
Junction temperature	T_J	-40		150	℃	

Storage Temperature	T_{stg}	-65		150	℃	

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rating condition for extended periods may affect device reliability.

[2] All voltage values, except for "Voltage between pin CANH and pin CANL", are with respect to GND terminal.

3. ESD Ratings (Electrostatic Discharge Protection)

Parameters		*Conditions*	*Value*	*Unit*	*Comments*
HBM	Human Body Model	CANH and CANL	±8	kV	According to AEC-Q100-002
		Other pins	±8	kV	According to AEC-Q100-002
CDM	Charged Device Model	All pins	±2	kV	According to AEC-Q100-011
MM	Machine Model	All pins	±600	V	According to JESD22-A115C
V_{TRAN}	ISO7637-2 transient per IEC 62228-3, on CANH and CANL	Pulse 1	-100	V	According to ISO7637-2
		Pulse 2a	75	V	According to ISO7637-2
		Pulse 3a	-150	V	According to ISO7637-2
		Pulse 3b	100	V	According to ISO7637-2

4. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Power Supply Voltage	VCC	4.5	5	5.5	V
I/O Level-Shifting Voltage	VIO	2.8	3.3	5.5	V
Operating Temperature	T_{opr}	-40		125	℃

5. Thermal Characteristics

Parameters	*Symbol*	*SOP8*	*DFN8*	*Unit*
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	145	50	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	50	40	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	45	20	℃/W

6. Specifications

6.1. Electrical Characteristics

V_{CC}=4.5V to 5.5V, V_{IO}=2.8 to 5.5V [1], Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{CC}=5V, V_{IO}=3.3V, Ta = 25℃.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	Supply voltage		4.5	-	5.5	V
I_{CC}	Supply current	Normal mode, recessive, $V_{TXD}=V_{IO}$ [2], V_S=0V	2.5	3.5	10	mA
		Normal mode, dominant, V_{TXD} =0V	20	40	70	mA
		Normal mode, dominant, V_{TXD} =0, short circuit on bus lines, -3V < (V_{CANH} = V_{CANL}) < 18V	2.5	56	110	mA
		Silent mode, V_{TXD} =V_{IO} [2]	0.1	1.95	2.5	mA
$V_{uvd(VCC)}$	Undervoltage detection voltage on pin VCC	Rising	3.5	4.15	4.5	V
		Falling	3.5	4.05	4.5	V
I/O level adapter supply; pin V_{IO}; only for NCA1051A-Q1						
V_{IO}	Supply voltage on pin VIO		2.8	-	5.5	V
I_{IO}	Supply current on pin VIO	Normal/ silent mode, recessive, $V_{TXD}=V_{IO}$	2	14	200	uA
		Normal mode, dominant, V_{TXD}=0V	-	175	1000	uA
$V_{uvd(VIO)}$	Undervoltage detection voltage on pin VIO	Rising	1.3	2.1	2.7	V
		Falling	1.3	2.0	2.7	V
Silent mode control input; pin S						
V_{IH}	High level input voltage		0.7*V_{IO} [2]	-	V_{IO}+0.3 [2]	V
V_{IL}	Low level input voltage		-0.3	-	0.3*V_{IO} [2]	V
I_{IH}	High level input current	$V_S=V_{IO}$ [2]	1	4.5	10	uA
I_{IL}	Low level input current	V_S=0V	-1	-	1	uA
CAN transmit data input; pin TXD						
V_{IH}	High level input voltage		0.7*V_{IO} [2]	-	V_{IO}+0.3 [2]	V
V_{IL}	Low level input voltage		-0.3	-	0.3*V_{IO} [2]	V
I_{IH}	High level input current	$V_{TXD}=V_{IO}$ [2]	-5	-	5	uA

I_{IL}	Low level input current	V_{TXD}=0V	-260	-150	-30	uA
C_i	Input capacitance	[3]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	High level output current	V_{RXD} = V_{IO} - 0.4V [2]	-8	-3	-1	mA
I_{OL}	Low level output current	V_{RXD} = 0.4V; bus dominant	2	5	12	mA
Bus lines; pins CANH and CANL; Driver						
$V_{OH(D)}$	CANH output voltage (Dominant)	V_{TXD} =0V, R_L=50Ω to 65Ω	2.75	3.4	4.5	V
$V_{OL(D)}$	CANL output voltage (Dominant)	V_{TXD} =0V, R_L=50Ω to 65Ω	0.5	1.2	2.25	V
$V_{OH(R)}$	CANH output voltage (Recessive)	Normal/ silent mode, no load	2	0.5*V_{CC}	3	V
$V_{OL(R)}$	CANL output voltage (Recessive)	Normal/ silent mode, no load	2	0.5*V_{CC}	3	V
$V_{OD(D)}$	Differential output voltage (Dominant)	Normal mode				
		R_L = 45Ω to 65Ω	1.5	-	3	V
		R_L = 45Ω to 70Ω	1.5	-	3.3	V
		R_L = 2240Ω	1.5	-	5	V
$V_{OD(R)}$	Differential output voltage (Recessive)	Normal mode, no load	-50	-	50	mV
V_{TXsym}	Transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}, [3] f_{TXD} = 1MHz, R_L=60Ω, C_{SPLIT} = 4.7nF, V_{CC} = 4.75V to 5.25V [4]	0.9*V_{CC}	-	1.1*V_{CC}	V
$I_{OSH(R)}$	CANH short-circuit output current, recessive	Normal mode, V_{CANH} = V_{CANL} = -27V to 32V	-5	-	5	mA
$I_{OSL(R)}$	CANL short-circuit output current, recessive	Normal mode, V_{CANH} = V_{CANL} = -27V to 32V	-5	-	5	mA
$I_{OSH(D)}$	CANH short-circuit output current, dominant	Normal mode, V_{CANH} = -15V to 18V, CANL open	-115	-70	115	mA
$I_{OSL(D)}$	CANL short-circuit output current, dominant	Normal mode, V_{CANL} = -15V to 18V, CANH open	-115	70	115	mA
Bus lines; pins CANH and CANL; Receiver						
$V_{ID(R)}$	Differential input threshold voltage, recessive	Normal/ silent mode -12V < V_{CANH} < 12V,	0.5	0.7	0.9	V

		-12V < V_{CANL} < 12V				
$V_{ID(D)}$	Differential input threshold voltage, dominant	Normal/ silent mode -12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V	0.5	0.8	0.9	V
V_{hys}	Differential input hysteresis voltage	Normal/ silent mode -12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V	50	80	200	mV
$V_{RX(R)}$	Receiver recessive voltage	Normal/ silent mode -12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V	-4	-	0.5	V
$V_{RX(D)}$	Receiver dominant voltage	Normal/ silent mode -12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V	0.9	-	9	V
$I_{LKG(OFF)}$	Power-off (unpowered) bus input leakage current	V_{CANH} = V_{CANL} = 5V, V_{CC} = V_{IO} = 0V	-5	-	5	uA
R_I	Input resistance	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V [3]	9	16	28	kΩ
$R_{I(match)}$	Input resistance matching	V_{CANH} = 5V, V_{CANL} = 5V, $R_{I(match)}$=2*(R_{CANH}-R_{CANL}) /(R_{CANH}+R_{CANL}) [3]	-1	-	1	%
R_{ID}	Differential input resistance	-2V ≤ V_{CANH} ≤ 7V, -2V ≤V_{CANL} ≤ 7V, R_{ID}=R_{CANH}+R_{CANL} [3]	19	33	52	kΩ
C_I	Input capacitance to ground	CANH or CANL [3]	-	13	-	pF
C_{ID}	Differential input	[3]	-	5	-	pF
Temperature detection						
T_{SD}	Thermal shutdown threshold	[3]	-	193	-	℃
$T_{SD(hys)}$	Thermal shutdown hysteresis	[3]	-	11	-	℃

[1] Only NCA1051A-Q1 has a VIO pin. For NCA1051N-Q1, the VIO input is internally connected to VCC.

[2] V_{IO}=V_{CC} for the version without VIO pin.

[3] Not tested in production; guaranteed by design.

[4] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 6-1, Figure 6-3.

6.2. Switching Electrical Characteristics

V_{CC} =4.5V~5.5V, V_{IO}=2.8~5.5V,Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Ta = 25℃

Symbol	Parameters	Comments	Min	Typ	Max	Unit
Driver						
$t_{d(TXD-bus, dom)}$	Delay time from TXD to bus dominant	Normal mode	-	40	-	ns
$t_{d(TXD-bus, rec)}$	Delay time from TXD to bus recessive	Normal mode	-	60	-	ns
$t_{r(bus)}$	Differential output signal rise time		-	45	-	ns
$t_{f(bus)}$	Differential output signal fall time		-	30	-	ns
$t_{bit(bus)}$	Transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	495	530	ns
		$t_{bit(TXD)}$ = 200 ns	155	195	210	ns
t_{TXD_DTO}	TXD dominant time-out time		0.8	2.2	5	ms
Receiver						
$t_{d(bus-RXD, dom)}$	Delay time from bus to RXD dominant	Normal/ silent mode	-	40	-	ns
$t_{d(bus-RXD, rec)}$	Delay time from bus to RXD recessive	Normal/ silent mode	-	35	-	ns
$t_{d(TXD-RXD, dom)}$	Delay time from TXD to RXD dominant	Normal mode	-	80	220	ns
$t_{d(TXD-RXD, rec)}$	Delay time from TXD to RXD recessive	Normal mode	-	95	220	ns
$t_{r(RXD)}$	RXD signal rise time		-	5	-	ns
$t_{f(RXD)}$	RXD signal fall time		-	5	-	ns
$t_{bit(RXD)}$	Bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	490	550	ns
		$t_{bit(TXD)}$ = 200 ns	120	190	220	ns
Δt_{rec}	Receiver timing symmetry	Distortion of RXD relative to bus				
		$t_{bit(TXD)}$ = 500 ns	-65	-35	40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-20	15	ns

6.3. Parameter Measurement Information

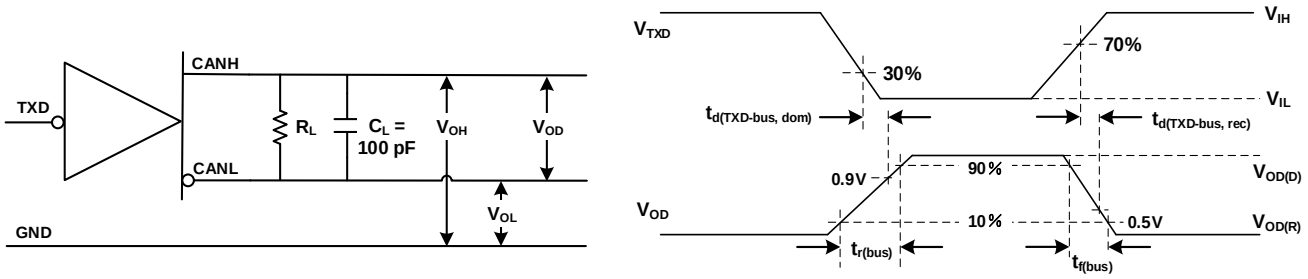


Figure 6-1 Driver Test Circuit and Voltage Waveforms

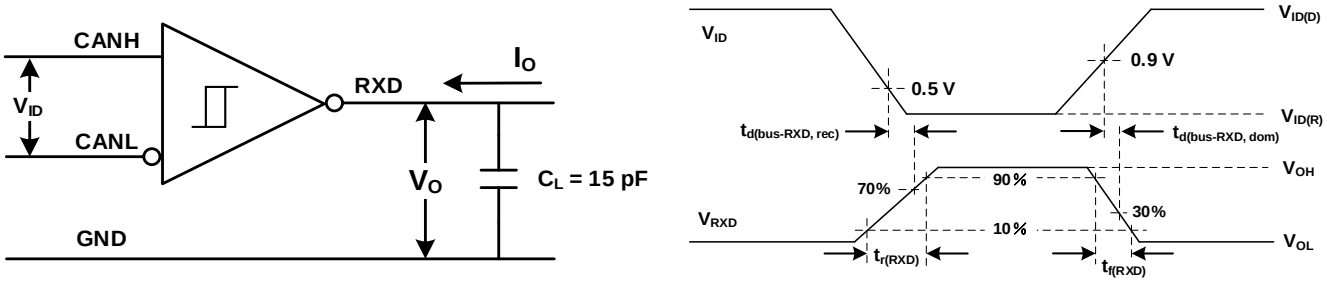


Figure 6-2 Receiver Test Circuit and Voltage Waveforms

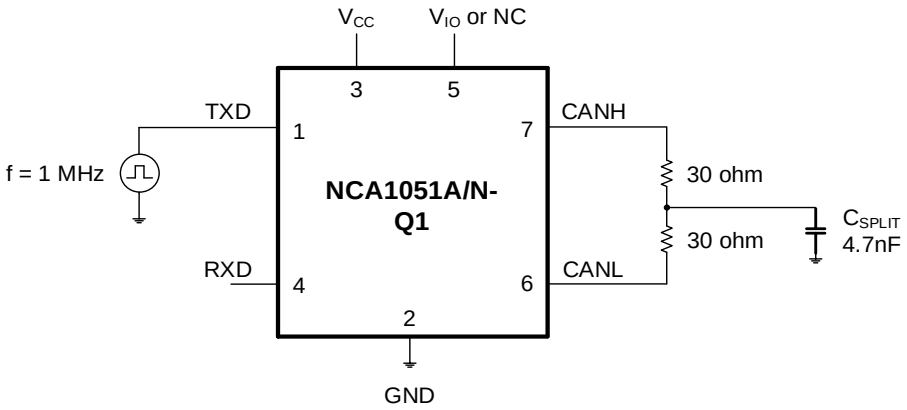


Figure 6-3 Transceiver Driver Symmetry Test Circuit

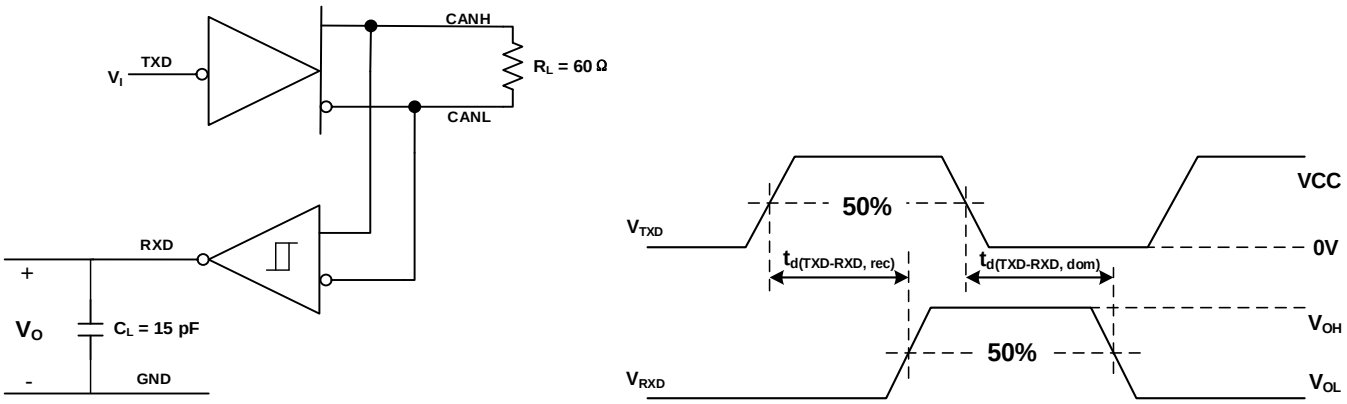


Figure 6-4 Loop Time Test Circuit and Voltage Waveforms

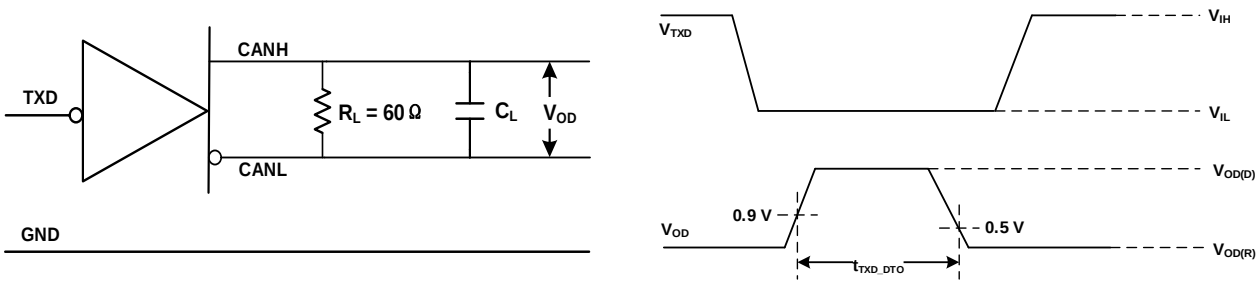


Figure 6-5 TXD Dominant Time-out Test Circuit and Voltage Waveforms

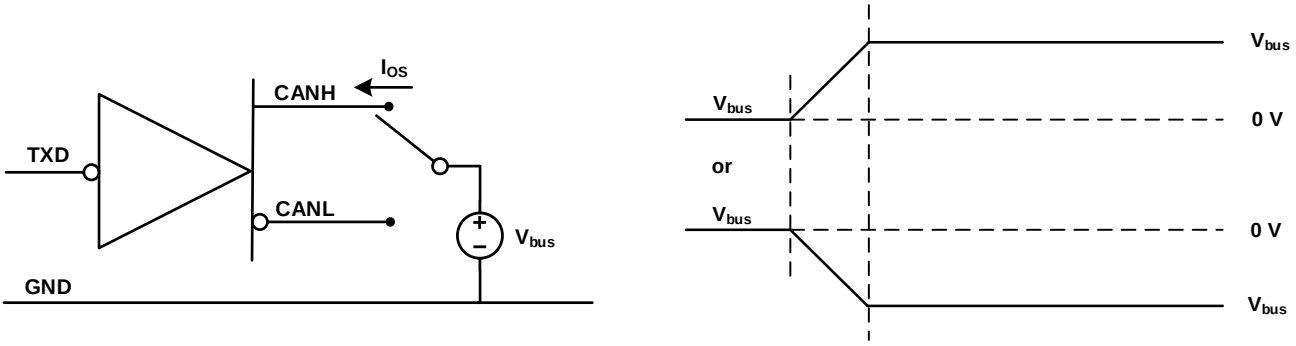


Figure 6-6 Driver Short-Circuit Current Test Circuit and Waveforms

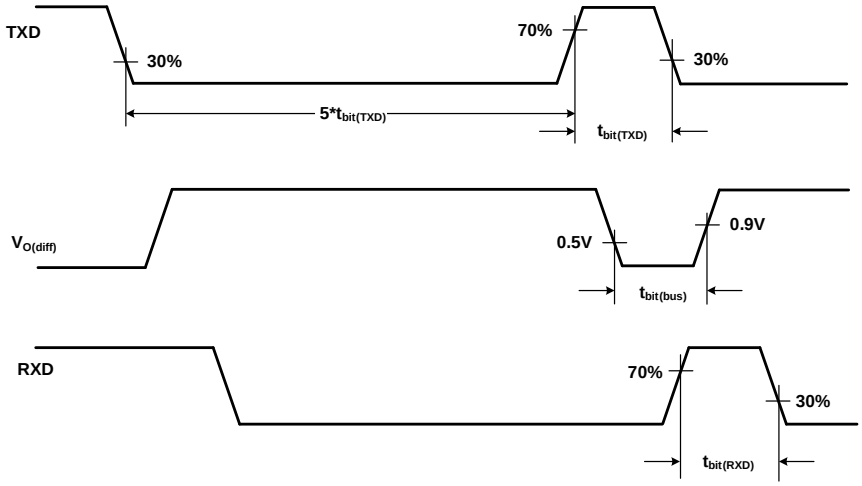
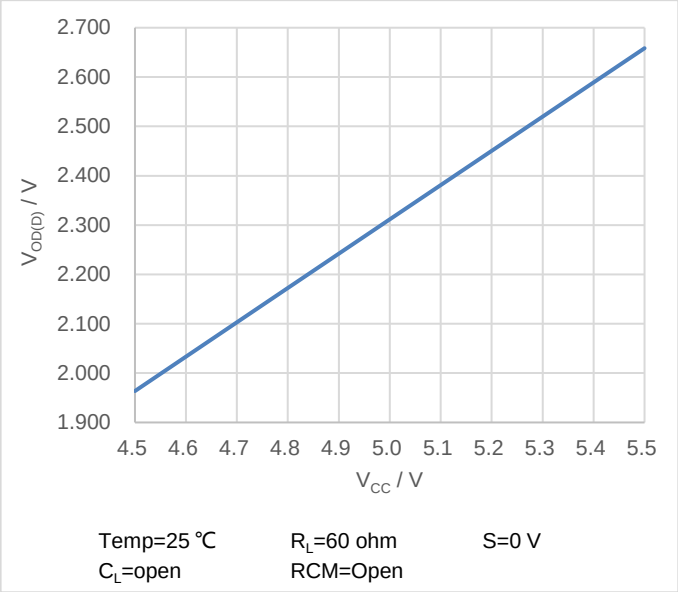


Figure 6-7 $t_{bit(RXD)}$ Test Circuit and Waveforms

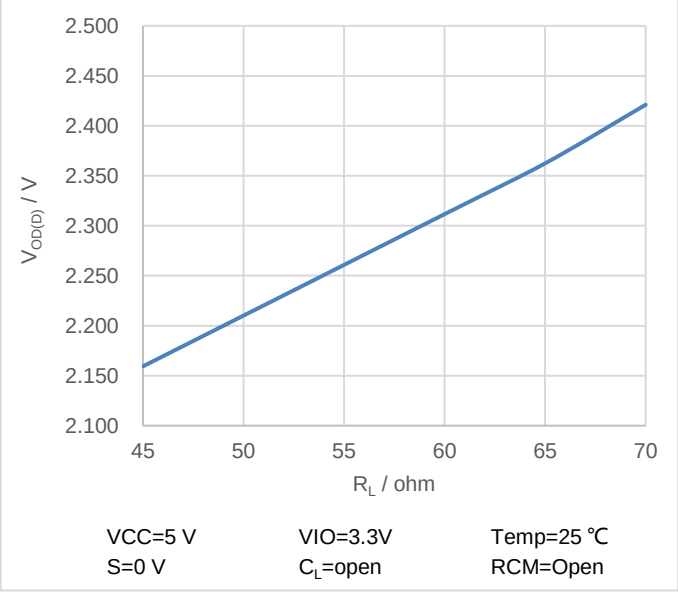
6.4. Typical Characteristics

V_{CC} =4.5V~5.5V, V_{IO}=2.8~5.5V, R_L=45~70 ohm, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, R_L=60 ohm, Ta = 25℃.



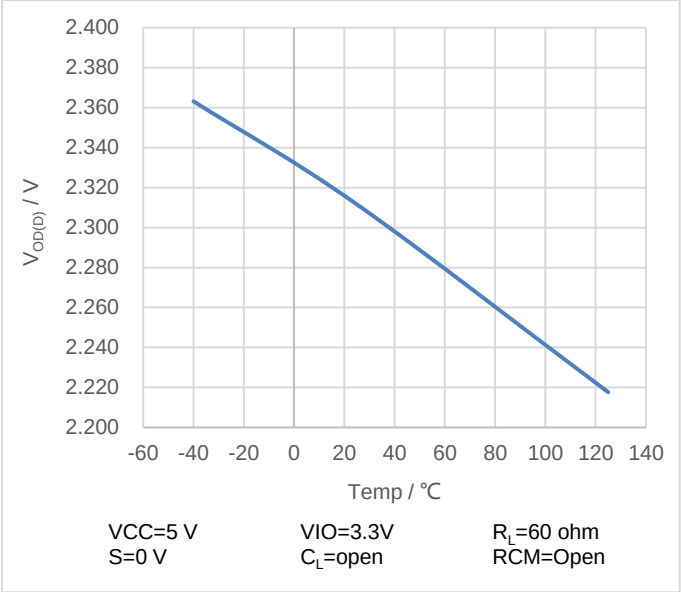
Temp=25 ℃ R_L=60 ohm S=0 V
C_L=open RCM=Open

Figure 6-8 $V_{OD(D)}$ vs VCC



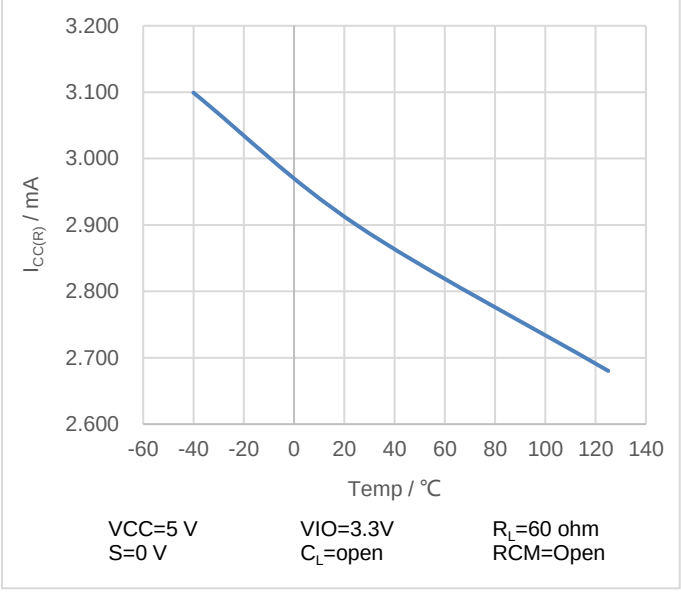
VCC=5 V VIO=3.3V Temp=25 ℃
S=0 V C_L=open RCM=Open

Figure 6-9 $V_{OD(D)}$ vs R_L



VCC=5 V VIO=3.3V R_L=60 ohm
S=0 V C_L=open RCM=Open

Figure 6-10 $V_{OD(D)}$ vs Temperature



VCC=5 V VIO=3.3V R_L=60 ohm
S=0 V C_L=open RCM=Open

Figure 6-11 $I_{CC(R)}$ vs Temperature

7. Function Description

7.1. Overview

The NCA1051A-Q1 is a CAN transceiver which fully compatible with the ISO11898-2 standard. The data rate of the NCA1051A-Q1 is up to 5Mbps, and it can support up to 110 CAN nodes. Meanwhile, the maximum transmission rate of the CAN bus is limited by the bus load, the quantity of nodes, the cable length, and other factors. The NCA1051A-Q1 has a ±30V input common-mode range, enabling reliable communication between bus nodes with large ground potential deviations.

Comprehensive protection features are designed to enhance the device and network robustness in harsh operating conditions. The transmit data dominant time-out function prevents the bus from lock-up by the faults on micro-controller. Moreover, the NCA1051A-Q1 provides thermal protection and short-circuit protection.

7.2. Functional Block Diagram

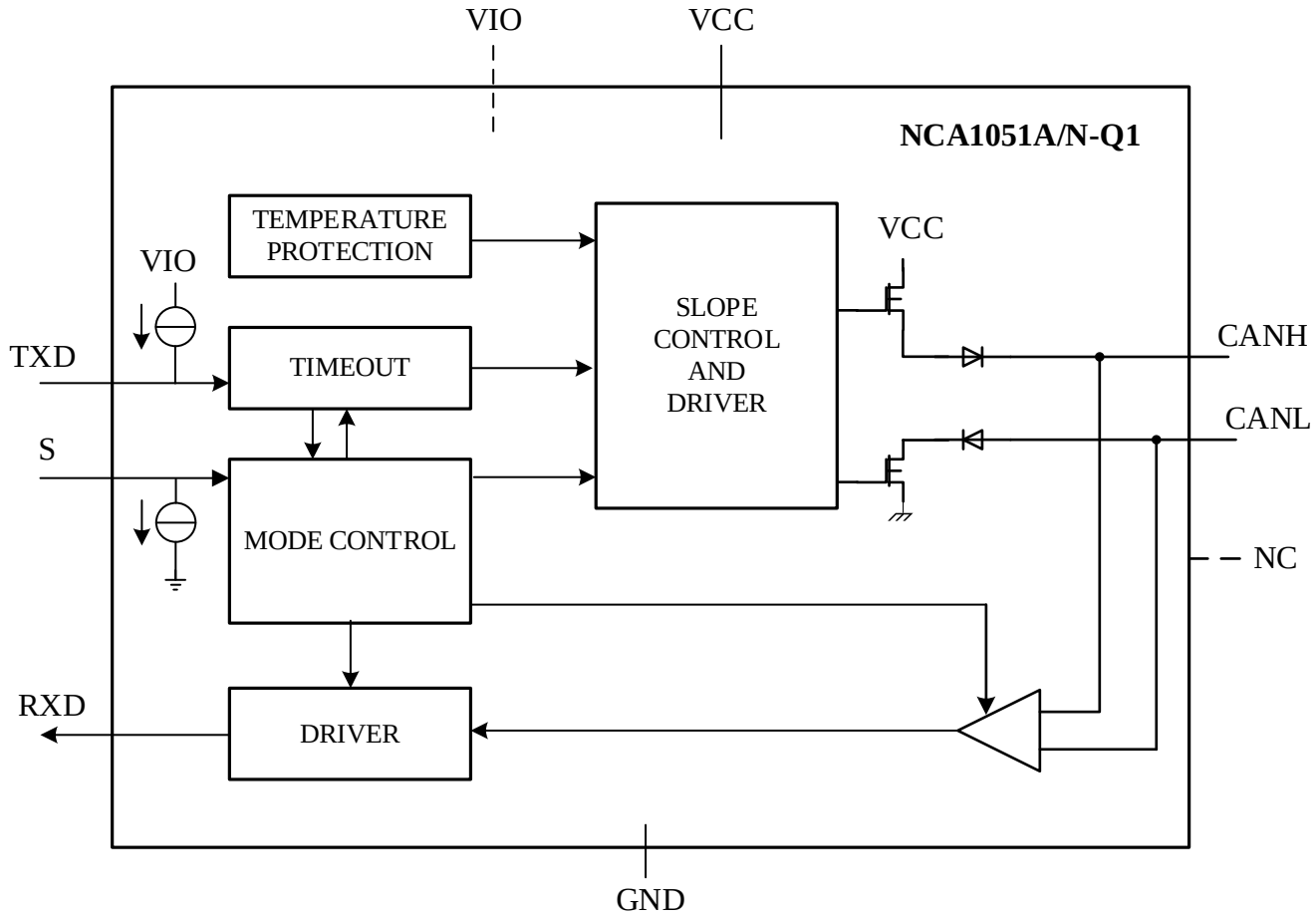


Figure 7-1 Block diagram of NCA1051A/N-Q1

7.3. Feature Description

7.3.1.TXD Dominant Time-Out Function (TXD DTO)

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

7.3.2. Undervoltage Detection on Pins VCC and VIO

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the VCC or VIO supply terminals.

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation within 50 µs.

Table 7-1 Undervoltage Lockout 5V Only Devices (NCA1051N-Q1)

VCC	Device State	Bus Output	RXD
>UV_{VCC}	Normal	Per TXD	Mirrors Bus[1]
<UV_{VCC}	Protected	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 7-2 Undervoltage Lockout I/O Level Shifting Devices (NCA1051A-Q1)

VCC	VIO	Device State	Bus Output	RXD
>UV_{VCC}	>UV_{VIO}	Normal	Per TXD	Mirrors Bus[1]
<UV_{VCC}	>UV_{VIO}	Protected	High Impedance	High (Recessive)
>UV_{VCC}	<UV_{VIO}	Protected	High Impedance	High Impedance
<UV_{VCC}	<UV_{VIO}	Protected	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

7.3.3. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

7.3.4. Internal Biasing of TXD and S Input Pins

Pin TXD has an internal pull-up to VIO, and pin S has an internal pull-down to GND. This ensures a safe, defined state in case one or both of these pins are left floating.

7.3.5. Over-Temperature Protection (OTP)

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{SD}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{SD} and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

7.3.6. Over-Current Protection (OCP)

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

7.4. VIO Supply Pin

Two versions of the NCA1051A-Q1 are available, only differing in the function of a single pin. Pin 5 is either a VIO supply pin or is not connected (NC).

Pin VIO should be connected to the microcontroller supply voltage (see Figure 8-1). This will adjust the signal levels of pins TXD, RXD and S to the I/O levels of the microcontroller. For versions of the NCA1051N-Q1 without a VIO pin, the VIO input is internally connected to VCC. This sets the signal levels of pins TXD, RXD and S to levels compatible with 5 V microcontrollers.

7.5. Device Functional Modes

The device has two main operating modes: Normal mode and Silent mode. Operating mode is selected via the S input pin.

Table 7-3 Operating Modes

S	Mode	Driver	Receiver	RXD Terminal
L	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State[1]
H	Silent Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State[1]

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

7.5.1.CAN Bus States

The CAN bus has two states during powered operation: dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic LOW on the TXD and RXD terminal. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_I of the receiver, corresponding to a logic HIGH on the TXD and RXD terminals.

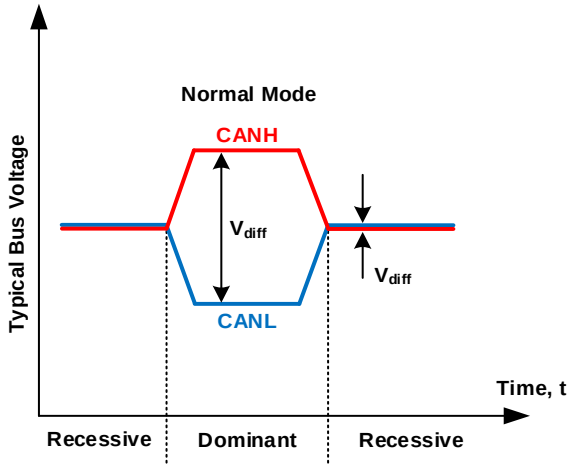


Figure 7-2 Bus States

7.5.2.Normal Mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 7-1). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible Electromagnetic Emission (EME).

7.5.3.Silent Mode

A HIGH level on pin S selects Silent mode. In Silent mode, the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

7.5.4.Driver and Receiver Function Tables

Table 7-4 Driver Function Table

Inputs		Outputs		Driven Bus State
S[1]	TXD[1] [2]	CANH[1]	CANL[1]	
L or Open	L	H	L	Dominant
	H or Open	Z	Z	Recessive
H	X	Z	Z	Recessive

[1] H= high level; L=low level; X=irrelevant; Z= common mode(recessive) bias to $V_{CC}/2$.

[2] Devices have an internal pull up to VCC or VIO on TXD terminal. If the TXD terminal is open, the terminal is pulled HIGH and the transmitter remain in recessive (non-driven) state.

Table 7-5 Receiver Function Table

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Terminal[1]
Normal or Silent	$V_{ID} \geq V_{ID(D)}$	Dominant	L
	$V_{ID(R)} < V_{ID} < V_{ID(D)}$	Uncertain	Uncertain
	$V_{ID} \leq V_{ID(R)}$	Recessive	H
	Open	Recessive	H

[1] H= high level; L=low level.

8. Application Information

8.1. Typical Application

The NCA1051A-Q1 requires a 0.1 µF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The Figure 8-1 and Figure 8-2 are the typical applications of NCA1051A-Q1.

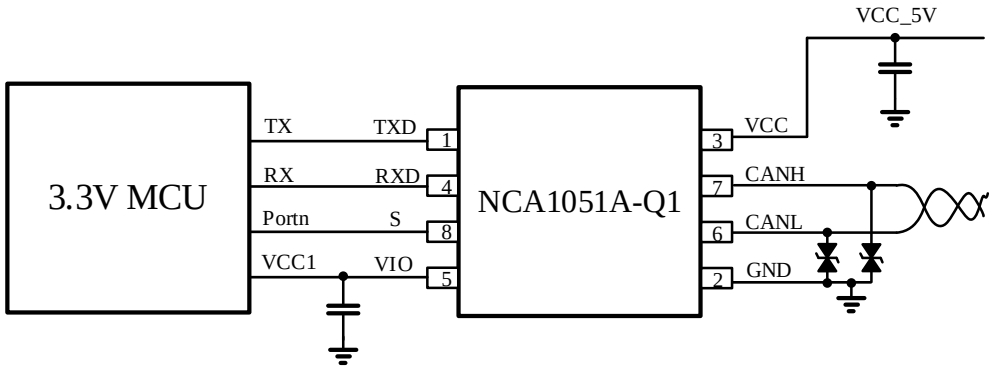


Figure 8-1 Typical CAN Bus Application Using 3.3V CAN Controller

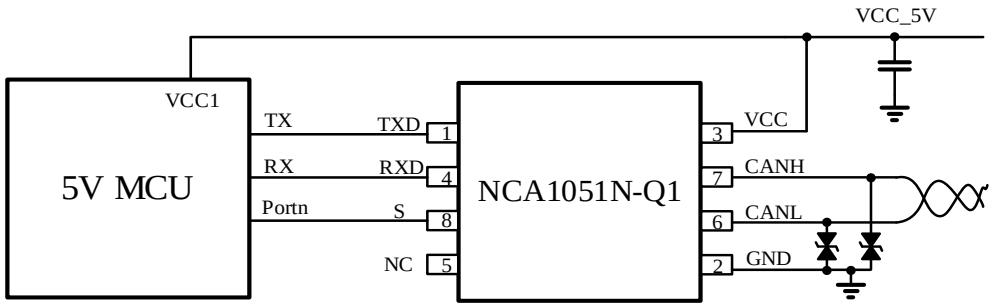
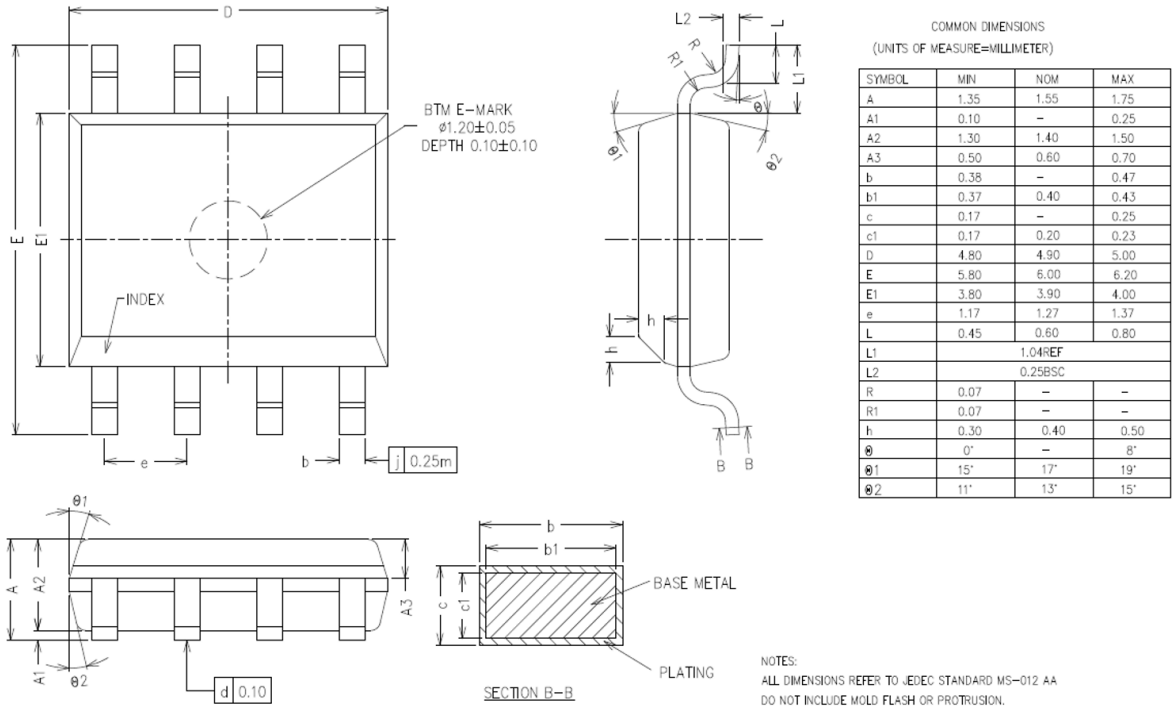


Figure 8-2 Typical CAN Bus Application Using 5V CAN Controller

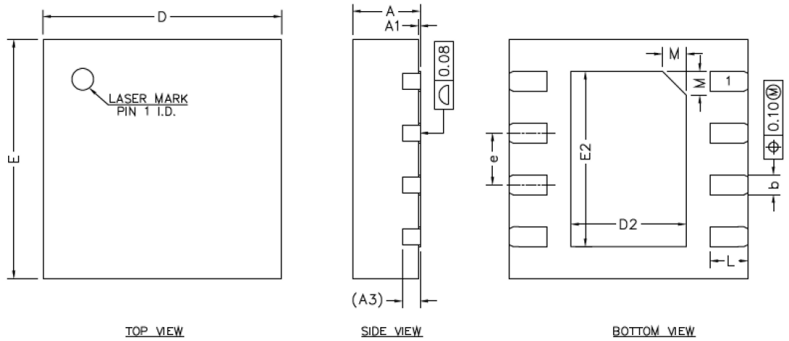
9. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

Figure 9-1 SOP8 Package Shape and Dimension



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.35	1.45	1.60
E2	2.10	2.20	2.35
e	0.55	0.65	0.75
L	0.425	0.475	0.525
M	0.30REF		

NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 9-2 DFN8 Package Shape and Dimension

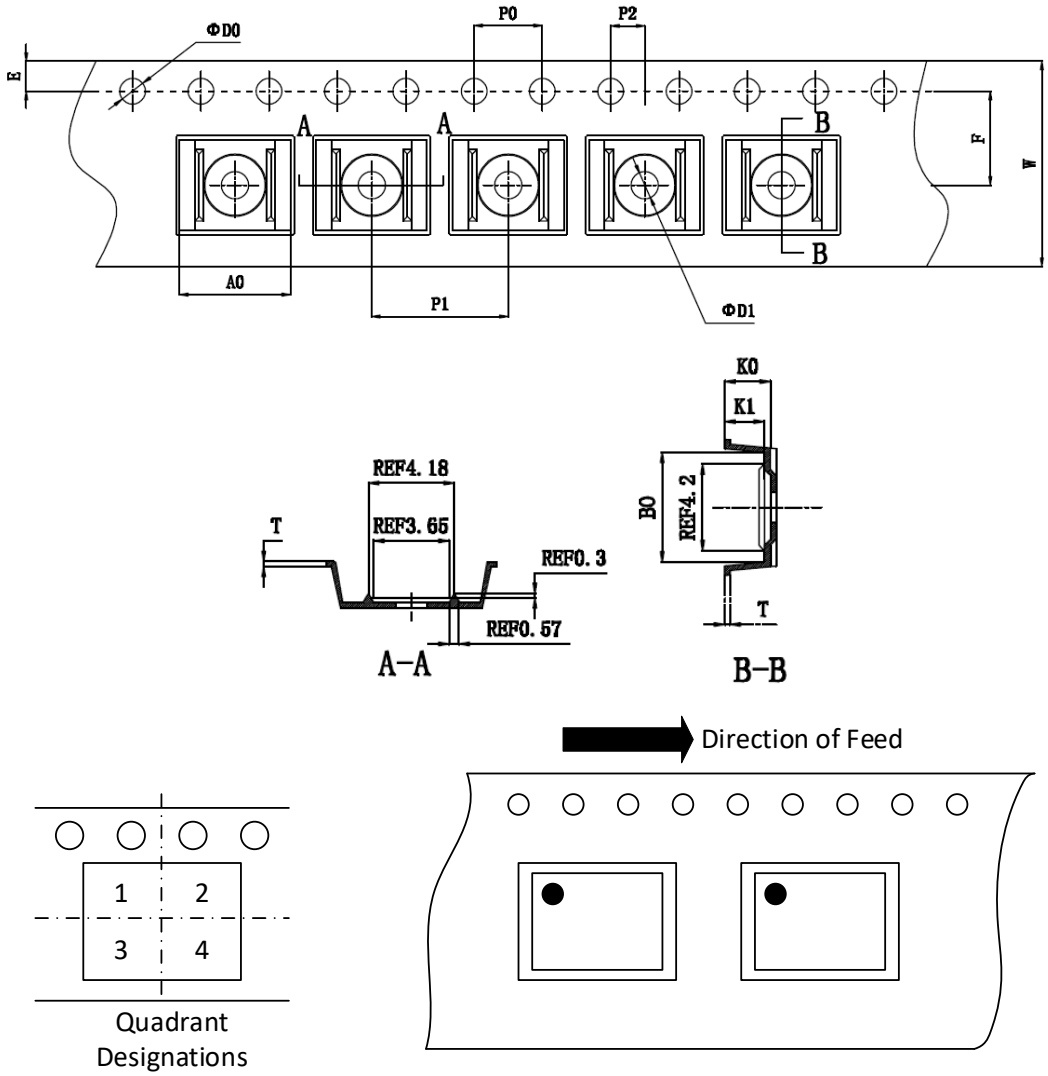
10. Order Information

Part Number	*Max Data Rate (Mbps)*	*Operation Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA1051A-Q1SPR	5	-40 to 125℃	1	SOP8	SOP8	2500
NCA1051A-Q1DNR	5	-40 to 125℃	1	DFN8	DFN8	5000
NCA1051N-Q1SPR	5	-40 to 125℃	1	SOP8	SOP8	2500
NCA1051N-Q1DNR	5	-40 to 125℃	1	DFN8	DFN8	5000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.						

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*
NCA1051A-Q1	Click here	Click here	Click here

12. Tape and Reel Information



Parameter	Dimension (mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Parameter	Dimension (mm)
W	12.00±0.30
P1	8.00±0.10
A0	6.50±0.10
B0	5.30±0.10
K0	2.20±0.10
K1	1.90±0.10
T	0.30±0.05

Figure 12-1 Tape and Reel Information of SOP8

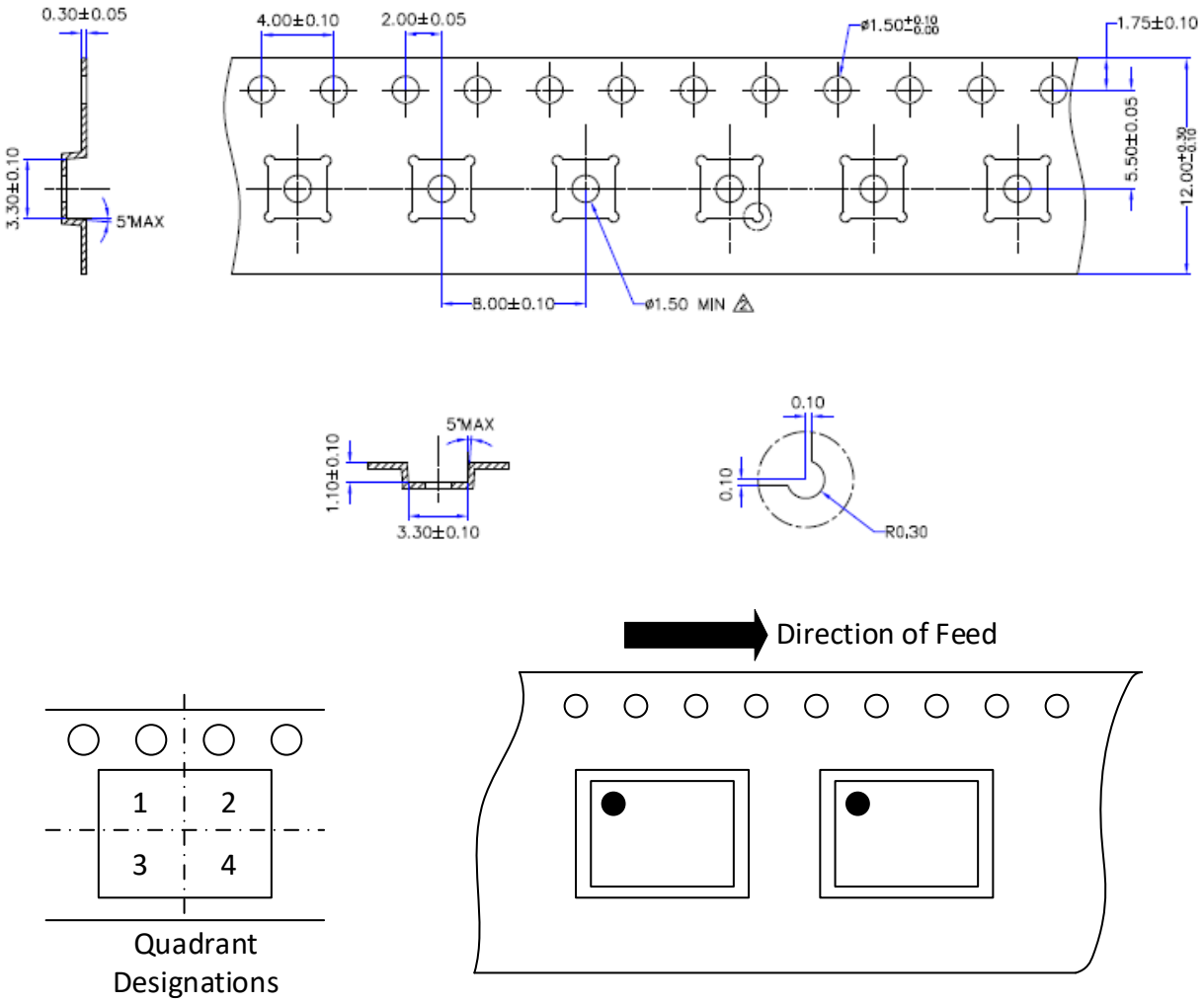


Figure 12-2 Tape and Reel Information of DFN8

13. Revision History

Revision	*Description*	*Date*
1.0	Initial version	2023/3/31
1.1	One-page information update; figure update; table format update; function description update	2023/8/25
1.2	Tape and reel information update; SPQ update	2023/11/20

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