NSD11416-Q1

1CH, 160mΩ, 40V, Fully Protected Automotive Low-side Switch

Datasheet (EN) 1.2

Product Overview

NSD11416-Q1 is a 160mΩ low-side switch with 48V clamp voltage for automotive applications. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnose function is built to indicate any faults when thermal shutdown and short circuit to ground conditions through an open-drain status output pin. This device operates in ambient temperatures from –40°C to 125°C.

Applications

- Automotive Relays
- Valves
- Solenoid drivers
- Lighting

Device Information

Part Number	Package	Body Size
NSD11416-Q1SPR	SO-8	4.9mm x 3.9mm
NSD11416-Q1STBR	SOT223	6.48mm x 3.38mm

Key Features

- AEC-Q100 (Grade 1) qualified for automotive application
- Drain current limitation: 2.5A
- 48V overvoltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block
  - Thermal shutdown diagnosis
  - Short circuit to ground diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection
- RoHS & REACH Compliance

Typical Application

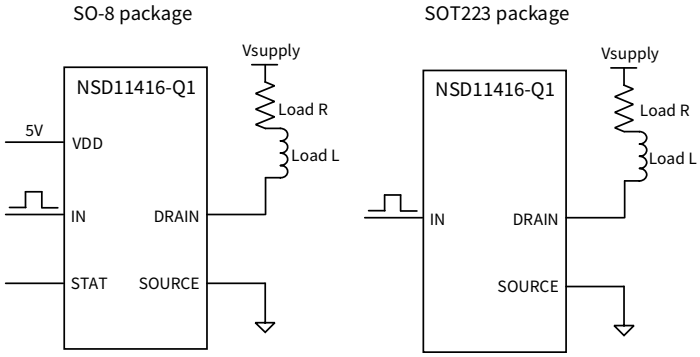


Figure 0.1 NSD11416-Q1 Typical Application

INDEX

1. PIN CONFIGURATION AND FUNCTIONS 3

2. BLOCK DIAGRAM 4

3. ABSOLUTE MAXIMUM RATINGS 5

4. ESD RATINGS 5

5. THERMAL INFORMATION 5

6. SPECIFICATIONS 6

6.1. ELECTRICAL CHARACTERISTICS 6
6.2. TYPICAL PERFORMANCE CHARACTERISTICS 8
6.2.1. True table 8
6.2.2. Switching characteristics 8

7. PROTECTIONS 8

7.1. CURRENT LIMITATION 8
7.2. THERMAL SHUTDOWN AND THERMAL SWING 8

8. APPLICATION INFORMATION 9

8.1. MCU I/O PROTECTION 10
8.2. THE VALUE OF STATUS PULLS UP RESISTOR 10

9. PACKAGE INFORMATION 11

9.1. SO-8 PACKAGE INFORMATION 11
9.2. SOT223 PACKAGE INFORMATION 11

10. PACKAGING INFORMATION 12

10.1. SO-8 PACKAGING INFORMATION 12
10.2. SOT223 PACKAGING INFORMATION 13

11. ORDERING INFORMATION 14

12. REVISION HISTORY 14

1. Pin Configuration and Functions

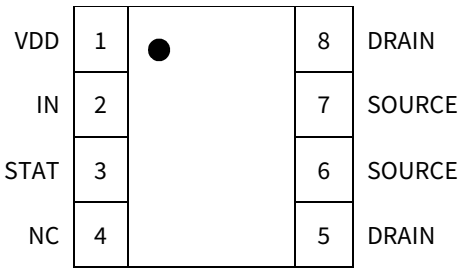


Figure 1.1 NSD11416-Q1SPR Pinout

Table 1.1 SO-8 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	VDD	Power supply pin.
2	IN	CMOS compatible, voltage-controlled input pin.
3	STAT	Open drain digital diagnostic pin.
4	NC	Not connect.
5, 8	DRAIN	PowerMOS drain.
6, 7	SOURCE	PowerMOS source and ground reference for the control section

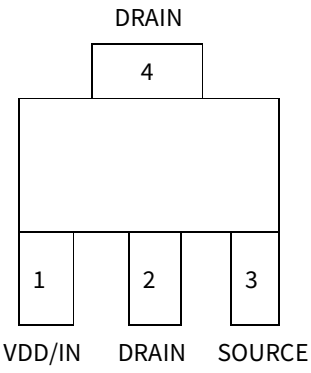


Figure 1.2 NSD11416-Q1STBR Pinout

Table 1.2 SOT223 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	VDD/IN	Power supply pin and voltage-controlled input pin, CMOS compatible.
2, 4	DRAIN	PowerMOS drain.
3	SOURCE	PowerMOS source.

2. Block diagram

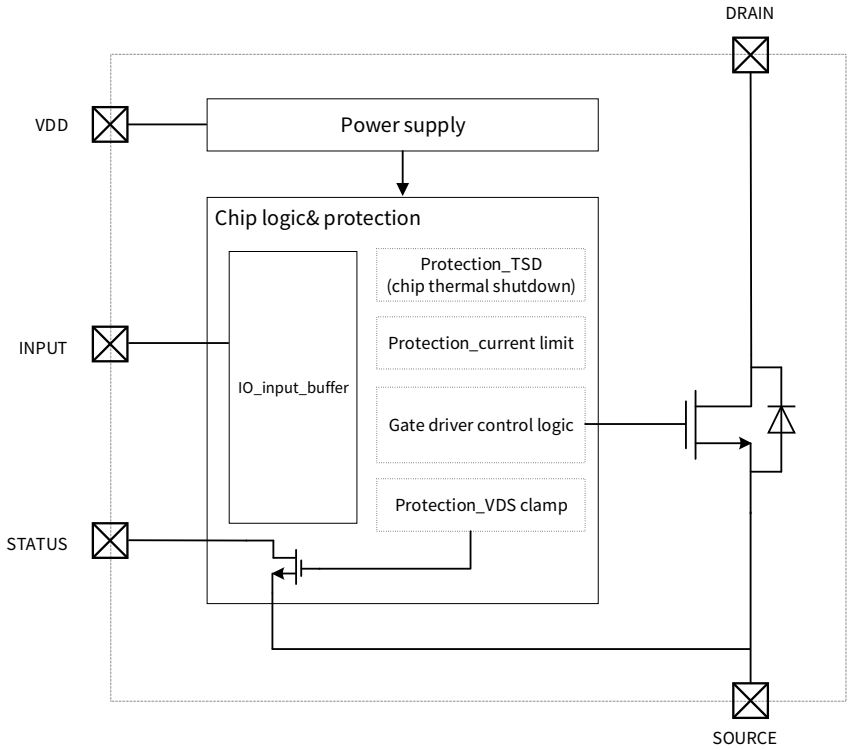


Figure 2.1 NSD11416-Q1SPR(SO-8) Block diagram

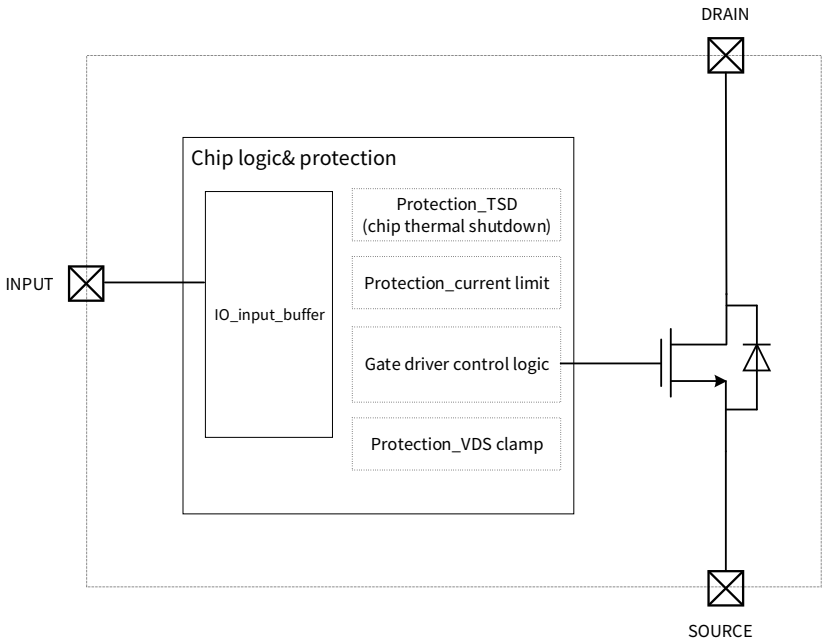


Figure 2.2 NSD11416- Q1STBR (SOT223) Block diagram

3. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Drain-to-Source Voltage	V_{DS}			Internally clamped	V
DC Drain Current	I_D			Thermal limited	A
VDD Pin Current	I_{VDD}	-1		10	mA
INPUT Pin Current	I_{IN}	-1		10	mA
STATUS Pin Current	I_{STAT}	-1		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C
Single pulse avalanche energy (L = 30mH; T_J = 150 °C; R_L = 0; I_{OUT} = 2.2A)	E_{AS}			37	mJ

4. ESD ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model, per AEC-Q100-002-RevD， $V_{ESD-HBM}$	±4000	V
	Charged-device model, per AEC-Q100-011-RevB， $V_{ESD-CDM}$	±750	V

5. Thermal Information

Parameters	Symbol	SO-8	SOT223	Unit
Junction-to-ambient Thermal Resistance	θ_{JA}	96.3	76.3	°C/W
Junction-to-top characterization parameter	ψ_{JT}	8.75	7.5	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	49.3	46.9	°C/W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layers board.

6. Specifications

6.1. Electrical Characteristics

(V_{DD} = V_{IN}= 4.5 V to 5.5 V, T_J=-40°C to 150°C. Unless otherwise noted.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power MOSFET						
Operating supply voltage	V_S	3.5	5	5.5	V	
ON-state resistance	R_{ON}		160		mΩ	I_D = 1 A; T_J = 25°C; V_{DD} = V_{IN} = 5 V
				320	mΩ	I_D = 1 A; T_J = 150°C; V_{DD} = V_{IN} = 5 V
Drain-source clamp voltage	V_{CLAMP}	46	48	56	V	V_{IN} = 0V, I_D = 1 A
Drain-source clamp threshold voltage	V_{CLTH}	40			V	V_{IN} = 0V, I_D = 2 mA
OFF-state output current	I_{DSS}	0		3	µA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 25°C
		0		5	µA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 125°C
Body diode forward voltage	V_{BD}		0.8		V	I_D = 1A; V_{IN} = 0 V
Input section (SOT223 package only)						
Supply current from input pin	I_{ISS}		30	65	µA	ON-state: V_{DD} = V_{IN} = 5 V; V_{DS} = 0 V
Input clamp voltage	V_{ICL}	5.5		8	V	I_S = 1 mA
			-0.7			I_S = -1 mA
Input threshold voltage	V_{INTH}	1		3.5	V	V_{DS} = V_{IN}; I_D = 1 mA
VDD (SO-8 package only)						
Operating supply current	I_S		10	25	µA	OFF-state; T_J = 25°C; V_{IN} = V_{DS} = 0 V;
			25	65	µA	ON-state; V_{IN} = 5 V; V_{DS} = 0 V
Supply clamp voltage	V_{SCL}	5.5		8	V	I_{SCL} = 1 mA
			-0.7			I_{SCL} = -1 mA
Logic Input (SO-8 package only)						
Low-level input voltage	V_{IL}			0.7	V	
Low-level input current	I_{IL}	1			µA	V_{IN} = 0.7V
High-level input voltage	V_{IH}	2.2			V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
High-level input current	I_{IH}			10	μA	V_{IN} = 2.2V
Input hysteresis voltage	$V_{I(hyst)}$	0.13			V	
Input clamp voltage	V_{ICL}	5.5		8	V	I_{IN} = 1 mA
			-0.7			I_{IN} = -1 mA
Status indicator (SO-8 package only)						
Status low output voltage	V_{STAT}			0.5	V	I_{STAT} = 1 mA
Status leakage current	I_{LSTAT}			10	μA	V_{STAT} = 5 V
Status pin input capacitance	C_{STAT}			100	pF	V_{STAT} = 5 V
Status clamp voltage	V_{STCL}	5.5		8	V	I_{STAT} = 1 mA
			-0.7			I_{STAT} = - 1 mA
short circuit to ground detection (SO8 package only)						
short circuit to ground OFF-state voltage detection threshold	V_{SCGTH}	1.1	1.2	1.4	V	V_{IN} = 0 V
Delay between INPUT falling edge and STATUS falling edge in short circuit to ground condition	$t_{d(STAT)}$		225		μs	I_{OUT} = 0 A
Switching characteristics						
Turn-on delay time	$t_{d(ON)}$		9		μs	R_L = 13 Ω, V_{CC} = 13 V
Turn-off delay time	$t_{d(OFF)}$		9		μs	R_L = 13 Ω, V_{CC} = 13 V
Rise time	t_r		9		μs	R_L = 13 Ω, V_{CC} = 13 V
Fall time	t_f		5		μs	R_L = 13 Ω, V_{CC} = 13 V
Switching energy losses at turn-on	W_{ON}		26		μJ	R_L = 13 Ω, V_{CC} = 13 V
Switching energy losses at turn-off	W_{OFF}		23		μJ	R_L = 13 Ω, V_{CC} = 13 V
Protection and diagnostics						
DC short-circuit current	I_{lim}	1.6	2.5	3	A	V_{DS} = 13 V, V_{DD} = V_{IN} = 5V
Shutdown temperature	T_{TSD}	150	175	200	°C	
Reset temperature	T_R	T_{RS} + 1	T_{RS} + 5		°C	
Thermal reset of STATUS	T_{RS}	135			°C	
Thermal hysteresis (T_{TSD} - T_R)	T_{HYST}		7		°C	
Dynamic temperature	ΔT_J		40		°C	T_J = -40°C, V_{CC} = 13V
Dynamic temperature hysteresis	$\Delta T_{J(HYS)}$		15		°C	

6.2. Typical Performance Characteristics

6.2.1. True table

Conditions	*Input*	*Drain*	*Status*
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Over-temperature limitation	L	H	H
	H	H	L
VDD under-voltage	L	H	X
	H	H	X
Short circuit to ground	L	L	L
	H	L	H

6.2.2. Switching characteristics

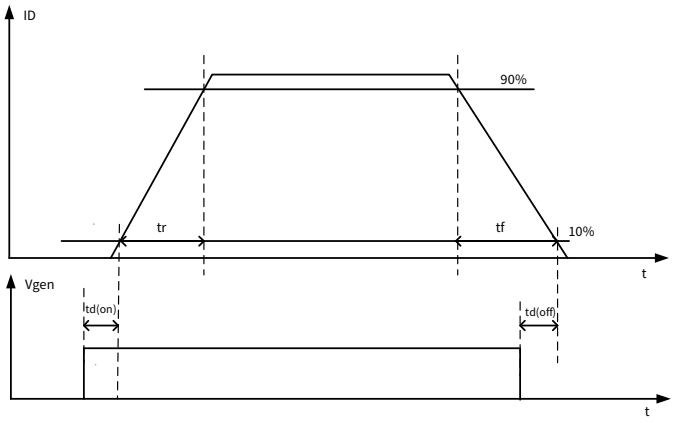


Figure 6.2.2 NSD11416-Q1 Switching Characteristics

7. Protections

7.1. Current Limitation

NSD11416-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to battery.

7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shut down the MOSFET when the hottest junction temperature exceeds the T_{TSD}, and the dynamic temperature protection is also to shut down the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔT_J.

8. Application information

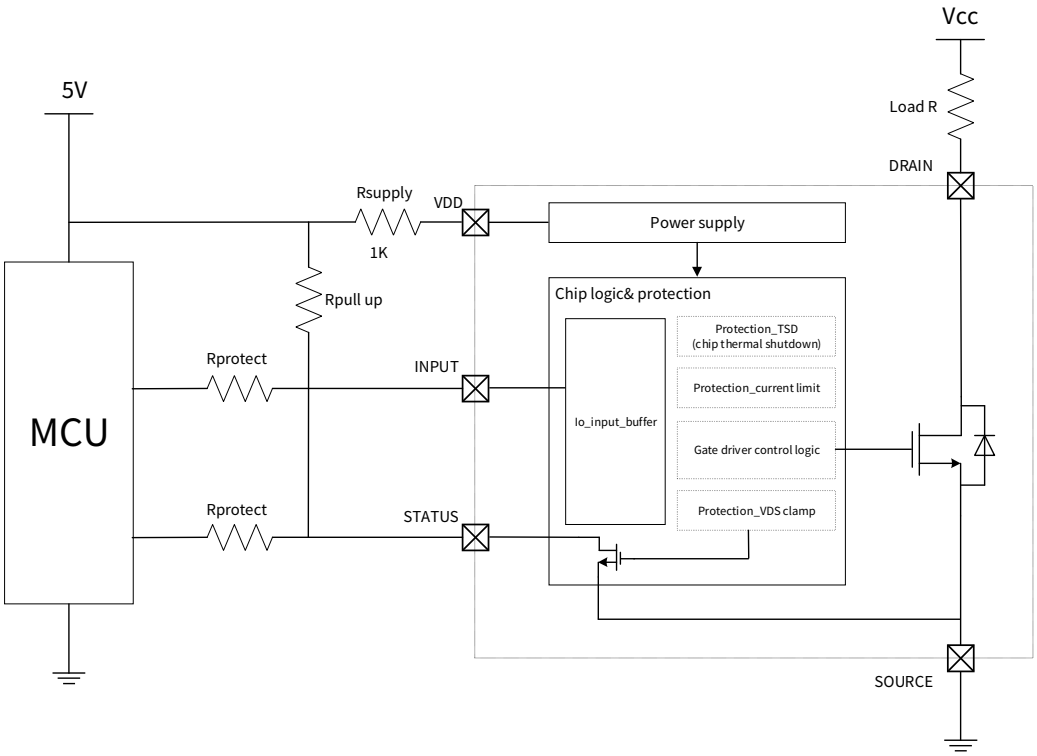


Figure 8.1 NSD11416-Q1SPR application schematic

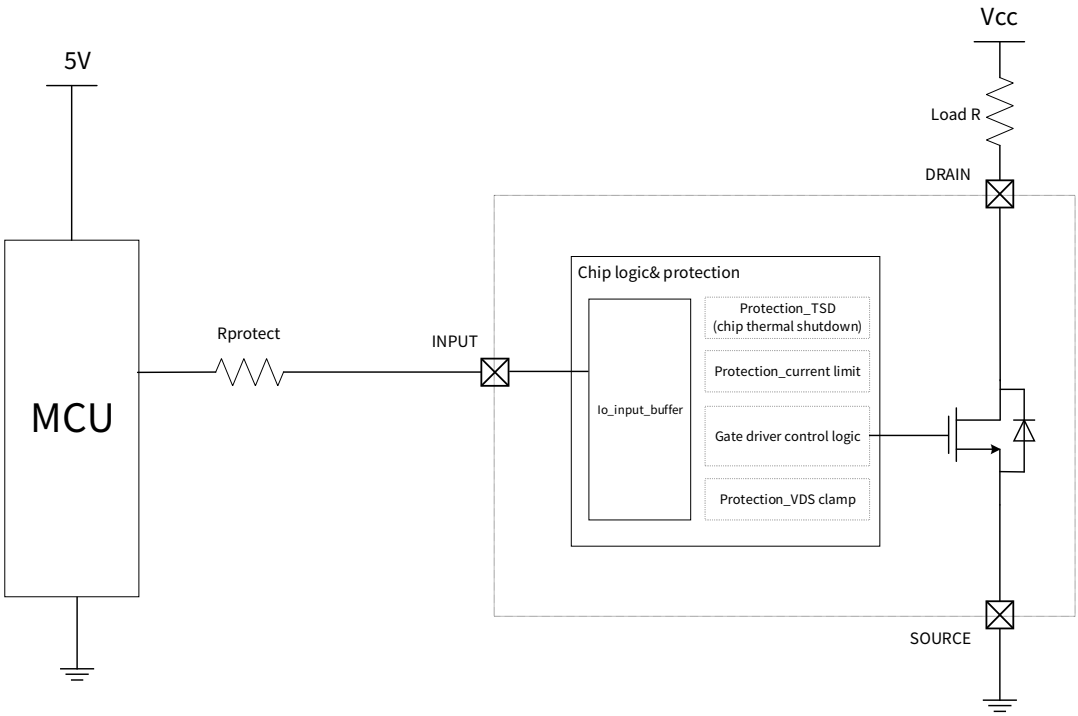


Figure 8.2 NSD11416-Q1STBR application schematic

8.1. MCU I/O protection

NSD11416 has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

$$\frac{0.7}{I_{latchup}} \le R_{prot} \le \frac{V_{MCU\_OUT} - V_{IH}}{I_{IHmax}}$$

Where $I_{latchup}$ is the MCU I/O latch up current, V_{MCU_OUT} is the output voltage of MCU I/O, V_{IH} is the High-level input voltage of NSD11416, I_{IH} is the High-level input current.

Let: $I_{latchup} \ge 20mA$; $V_{MCU\_OUT} \ge 4.5V$, so $35\Omega \le R_{prot} \le 15k\Omega$, the recommended value is $1k\Omega$. The supply resistor is the same.

8.2. The value of STATUS pulls up resistor

Because the STATUS pin is open drain output, a pull up resister is needed to fix the high voltage during normal operation. When the fault occurs, the voltage level of STATUS is pulled down by the internal MOSFET on. The value of pull up resistor can be calculated by the formula as shown below:

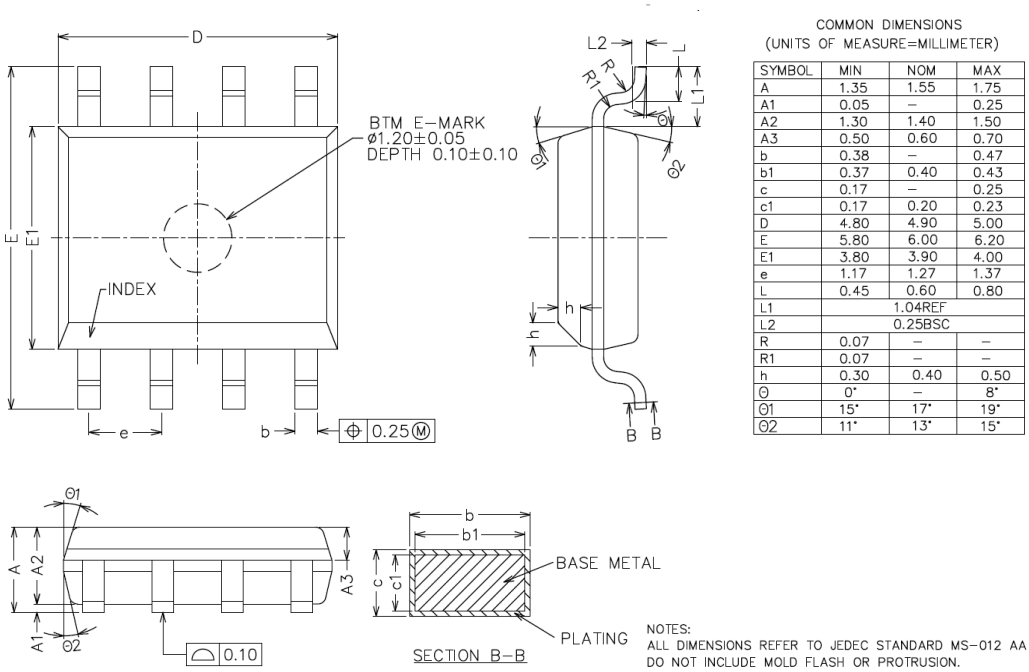
$$\left(\frac{V_{pull\text{-}up}}{V_{OL}} - 1\right) \cdot R_{on} < R_{pull\text{-}up} < \frac{V_{pull\text{-}up} - V_{OH}}{I_{leak}}$$

Where V_{pullup} is the minimum of pull-up supply, V_{OL} is the maximum of MCU logic low, R_{on} is the on resistance of the MOSFET of STATUS pin, V_{OH} is the minimum of MCU logic high, I_{leak} is the maximum leakage current of STATUS pin.

Let: $V_{pullup} = 4.5V$; $Ron = V_{STAT}/I_{STAT} = 500\Omega$, $V_{OL} = 0.9V$; $V_{OH} = 2.1V$; $I_{leak} = 10uA$, so $2k\Omega \le R_{pullup} \le 240k\Omega$.

9. Package Information

9.1. SO-8 package information

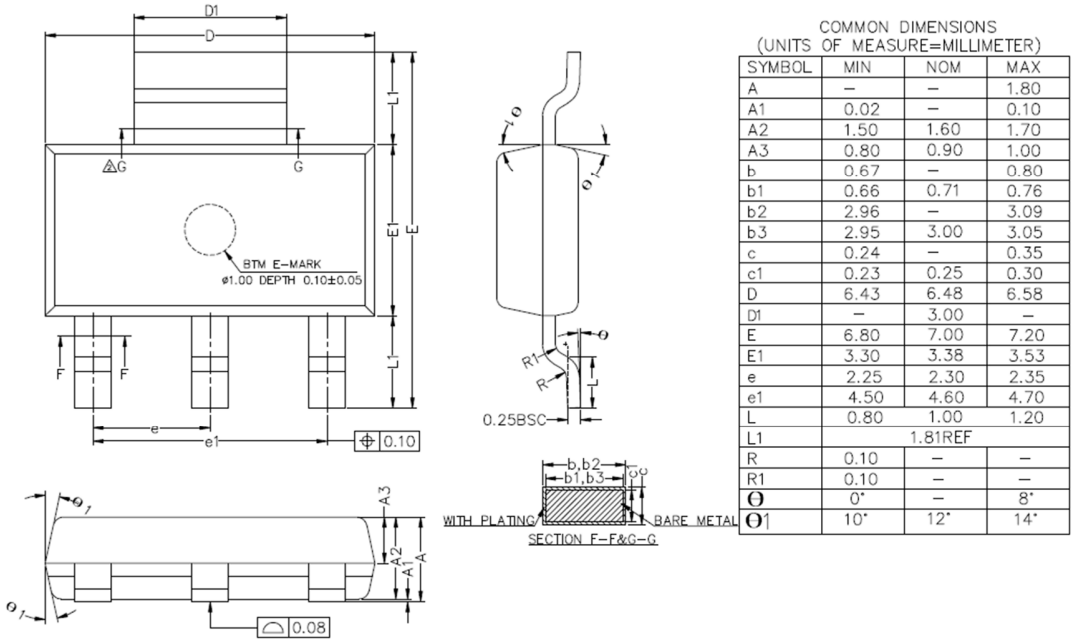


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
Θ	0°	–	8°
Θ1	15°	17°	19°
Θ2	11°	13°	15°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

9.2. SOT223 package information

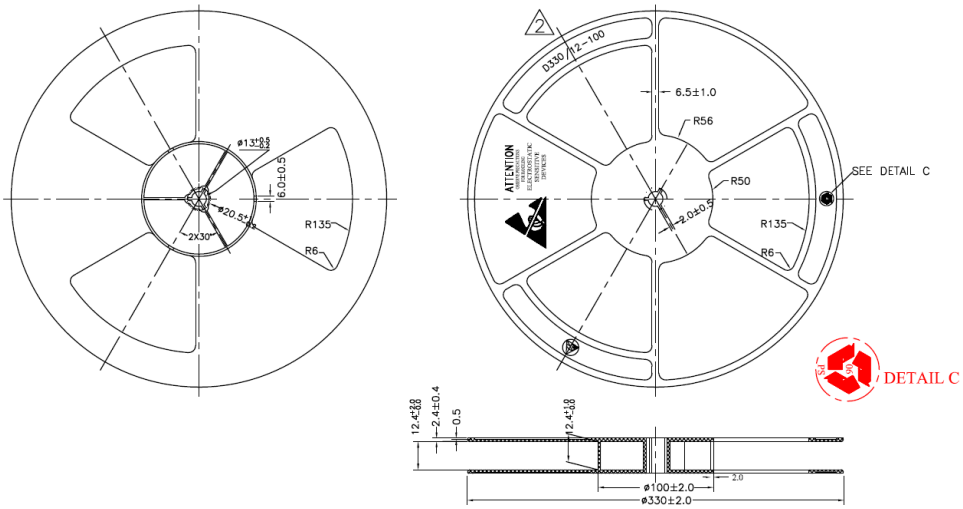


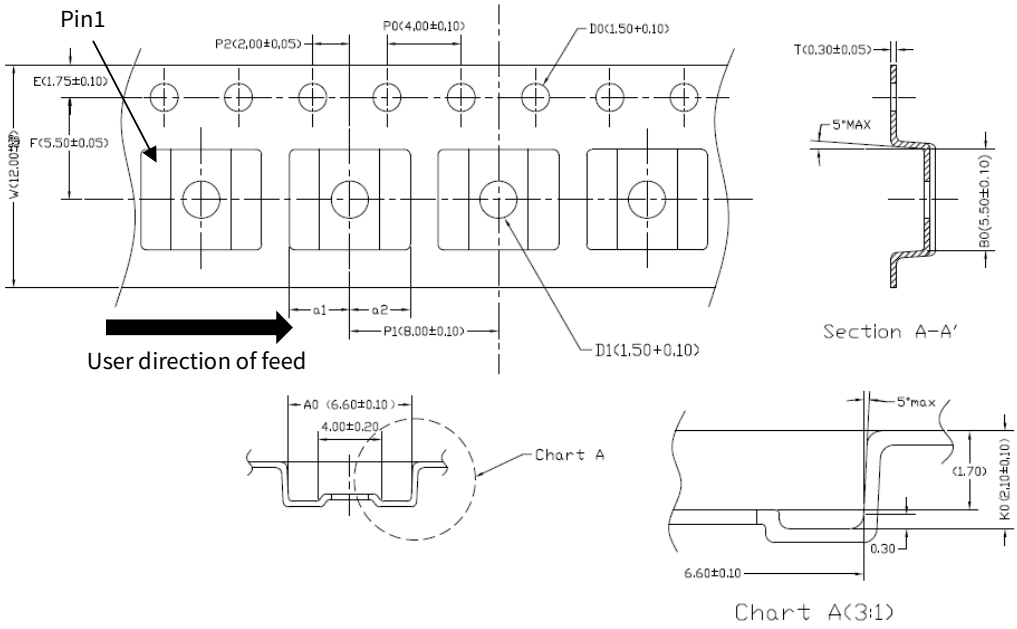
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.80
A1	0.02	–	0.10
A2	1.50	1.60	1.70
A3	0.80	0.90	1.00
b	0.67	–	0.80
b1	0.66	0.71	0.76
b2	2.96	–	3.09
b3	2.95	3.00	3.05
c	0.24	–	0.35
c1	0.23	0.25	0.30
D	6.43	6.48	6.58
D1	–	3.00	–
E	6.80	7.00	7.20
E1	3.30	3.38	3.53
e	2.25	2.30	2.35
e1	4.50	4.60	4.70
L	0.80	1.00	1.20
L1	1.81REF		
R	0.10	–	–
R1	0.10	–	–
Θ	0°	–	8°
Θ1	10°	12°	14°

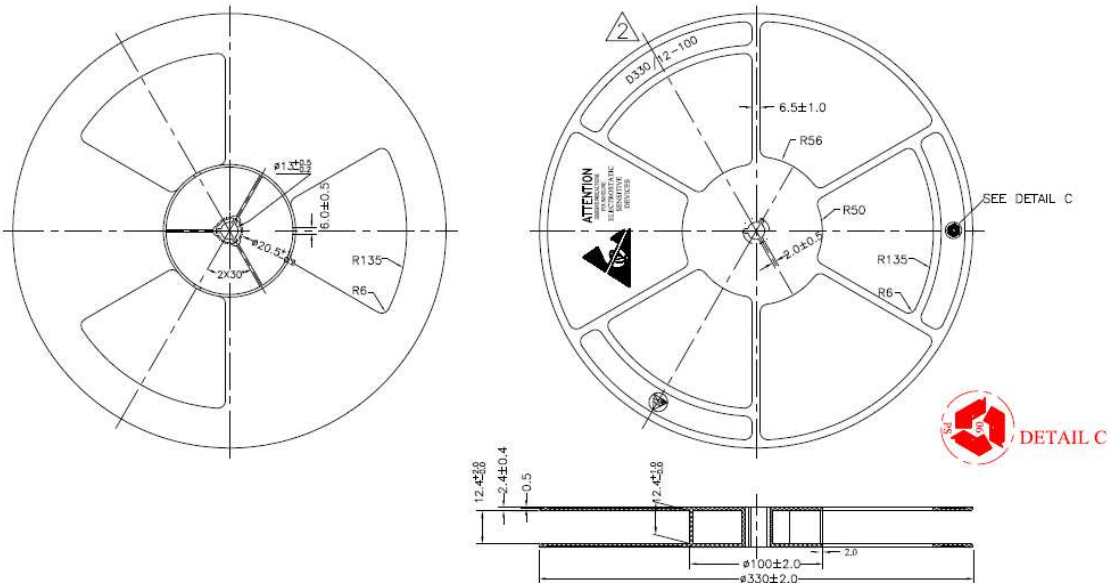
10. Packaging Information

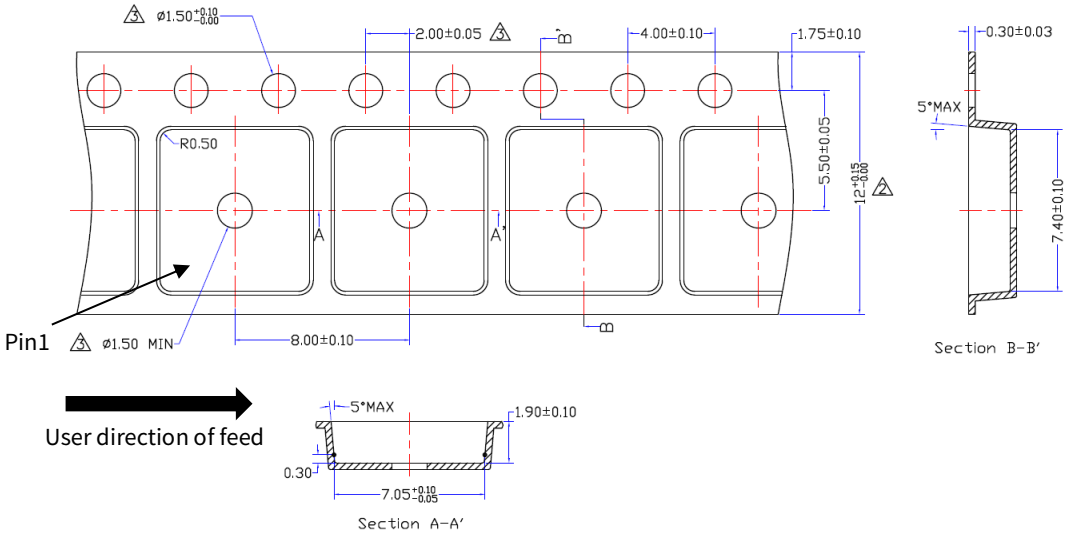
10.1. SO-8 packaging information





10.2.SOT223 packaging information





11. Ordering Information

Part Number	Package	MSL	SPQ
NSD11416-Q1SPR	SO-8	3	2500
NSD11416-Q1STBR	SOT223	3	2500
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.			

12. Revision History

Revision	Description	Date
1.0	Initial version	2024/1/31
1.1	Update description	2024/3/15
1.2	Update “short circuit to ground OFF-state voltage detection threshold” max value	2024/4/7

IMPORTANT NOTICE

The information given in this document (the “Document”) shall in no event be regarded as any warranty or authorization of, express or implied, including but not limited to accuracy, completeness, merchantability, fitness for a particular purpose or infringement of any third party’s intellectual property rights.

Users of this Document shall be solely responsible for the use of NOVOSENSE’s products and applications, and for the safety thereof. Users shall comply with all laws, regulations and requirements related to NOVOSENSE’s products and applications, although information or support related to any application may still be provided by NOVOSENSE.

This Document is provided on an “AS IS” basis, and is intended only for skilled developers designing with NOVOSENSE’ products. NOVOSENSE reserves the rights to make corrections, modifications, enhancements, improvements or other changes to the products and services provided without notice. NOVOSENSE authorizes users to use this Document exclusively for the development of relevant applications or systems designed to integrate NOVOSENSE’s products. No license to any intellectual property rights of NOVOSENSE is granted by implication or otherwise. Using this Document for any other purpose, or any unauthorized reproduction or display of this Document is strictly prohibited. In no event shall NOVOSENSE be liable for any claims, damages, costs, losses or liabilities arising out of or in connection with this Document or the use of this Document.

For further information on applications, products and technologies, please contact NOVOSENSE (www.novosns.com).

Suzhou NOVOSENSE Microelectronics Co., Ltd