NST175-Q1
Automotive Level Temperature Sensor with SMBus and I2C Interface
Datasheet (EN) 1.0

Product Overview

The NST175-Q1 is a low-power, high precision digital temperature sensor compatible with SMBus and I²C interfaces, supports up to 27 device addresses and provides SMBus Reset and Alert functions. The typical accuracy of NST175-Q1 is ±0.2°C without requiring calibration or external component signal conditioning, it is highly linear and does not require complex calculations or look-up tables to derive temperature. The device has a 12-bit analog-to-digital converter (ADC) inside, with a maximum resolution of 0.0625°C. The NST175-Q1 is available in SOP(8) package and MSOP(8) package.

NST175-Q1 device works over a temperature range of –40°C to 125°C, which makes it suitable for onboard applications in automotive, industrial, and consumer markets.

Key Features

- High Accuracy over –40°C to 125°C Wide Temperature Range:
  - -20°C ~ 85°C: ±0.2°C (Typ.) ±0.5°C (Max.)
  - -40°C ~125°C: ±0.5°C (Typ.) ±1°C (Max.)
- Resolution Range from 9 to 12Bits, User Configurable, up to 0.0625°C
- Power up Defaults Permit Stand-Alone Operation as Thermostat
- Supports up to 27 Device Addresses
- Supply Operation Range from 1.62V to 5.5V
- Operating Current: 27μA (Typical)
- Shutdown Current: 0.2μA (Typical)
- Digital Interface: SMBus, I²C
- Package: MSOP(8), SOP(8)
- AEC-Q100 Qualified

Applications

- Airbag Control Units
- HID Lamps
- Engine Control Units
- Battery Control Units
- Climate Controls
- Infotainment Processor Management
- Airflow Sensors
- Water Pumps

Device Information

Part Number	Package	Body Size
NST175H-Q1MSR	MSOP(8)	3.00mm × 3.00mm
NST175H-Q1SPR	SOP(8)	4.90mm × 3.91mm

Typical Application

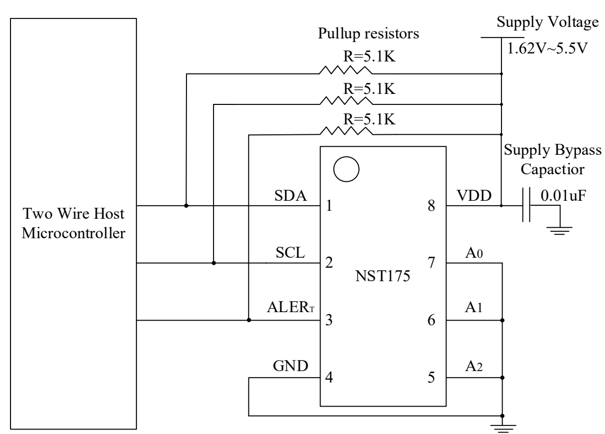

Figure 1 The Typical Application of NST175-Q1

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1. Pin Configuration and Functions

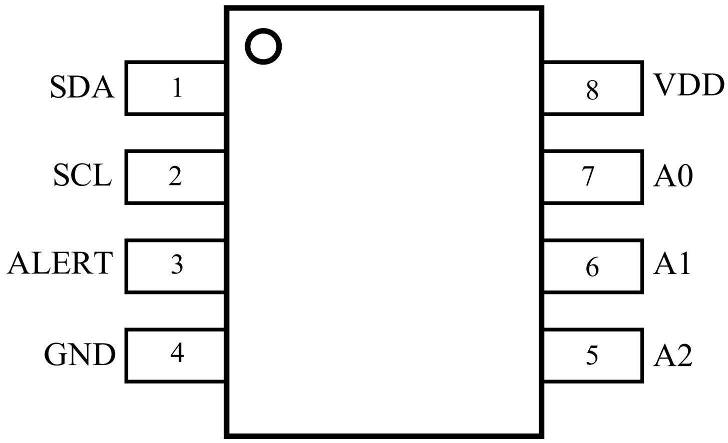


Figure 1.1 NST175-Q1 Pin Configuration (Top View)

Table 1.1 NST175-Q1 Pin Function Description

Pinout No.	Pinout Name	Type	Description
1	SDA	I/O	Serial data. Open-drain output, requires a pull up resistor
2	SCL	I	Serial clock. Open-drain output, requires a pull up resistor
3	ALERT	O	Over temperature alert. Open-drain output, requires a pull up resistor
4	GND	GND	Ground
5	A2	I	Address pin (Connect to GND, VDD or leave these pins floating)
6	A1		
7	A0		
8	VDD	Power	Supply voltage, 1.62V to 5.5V

2. Specifications

2.1. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage Pin (VDD)	VDD	-0.3		6.5	V	
Voltage at A0, A1 and A2 Pins	A0, A1, A2	-0.3		6.5	V	
Voltage at OS, SCL and SDA Pins	ALERT, SCL, SDA	-0.3		6.5	V	
Storage Temperature		-60		155	°C	
Operation Temperature	$TB_{operation}$	-40		125	°C	
Maximum Junction Temperature				155	°C	

2.2. ESD Ratings

Parameters	Symbol	Value	Unit
Electrostatic Discharge(ESD)	Human Body Model (HBM)[1]	±4000	V
	Charged Device Model (CDM)[2]	±2000	V

(1) Refer to AEC-Q100-002.

(2) Refer to AEC-Q100-011.

2.3. Electrical Characteristics

at TA = -40°C to +125°C and VDD = +1.62V to +5.5V, R_{pu} = 5.1kohm, unless otherwise noted.

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply						
Supply Voltage Range	VDD	1.62	3.3	5.5	V	
Supply Sensitivity			13	80	m°C/V	from -40°C to 125°C
Operation Current	R_{CONV}		27	40	µA	
Shutdown Current	I_{SD}		0.2	2	µA	Serial Bus Inactive
			10		µA	Serial Bus active, i2c Frequency=400kHz
Temperature Range and Resolution						
Temperature Range		-40		125	°C	
Resolution			0.0625		°C	
Accuracy			±0.2	±0.5	°C	from -20°C to 85°C
			±0.5	±1	°C	from -40°C to 125°C
Conversion Time	T_{CONV}		30	40	ms	
ALERT Output Saturation Voltage				0.5	V	I_{OUT} = 4mA
Timeout Time	$T_{TIMEOUT}$		54		ms	

Parameters	***Symbol***	***Min***	***Typ***	***Max***	***Unit***	***Comments***
Supply						
High-level Input Voltage	V_H	VDD*0.7		VDD+0.3	V	
Low-level Input Voltage	V_L	-0.3		VDD*0.3	V	
High-level Input Current				1	µA	
Low-level Input Current				-1	µA	
Digital Inputs Capacitance	C_{IN}		5		pF	
Output Leakage Current	I_{OH}			1	µA	V_{OH}=5V
Low-level Output Voltage	V_{OL}			0.4	V	I_{OL}= 3mA
Thermal Response						
Thermal Response Time			0.9		s	Stirred Oil Thermal Setting to 63% of Final Value
Drift						
Drift (1)			0.03		°C	

(1) Drift information is based on a 1000-hour stress test at +125°C with VDD = 5.5V.

2.4. I²C Timing characteristics

at TA = +25°C and VDD = +1.62V to +5.5V, Rpu = 5.1kohm, unless otherwise noted.

Parameters	**Symbol**	**STARDARD MODE**		**FAST MODE**		**HIGH-SPEED MODE**		**Unit**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
SCL operating frequency	F_{SCL}	0.001	0.1	0.001	0.4	0.001	2	MHz
Bus-free time between STOP and START conditions	$t_{(BUF)}$	4.7	-	1300	-	160	-	ns
Hold time after repeated START condition, after this period, the first clock is generated	$t_{(HDSTA)}$	4000	-	600	-	160	-	ns
Repeated START condition setup time	$t_{(SUSTA)}$	4700	-	600	-	160	-	ns
STOP condition setup time	$t_{(SUSTO)}$	4000	-	600	-	160	-	ns
Data hold time	$t_{(HDDAT)}$	0	-	4	-	4	120	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	10	-	ns
SCL clock low period	$t_{(LOW)}$	4700	-	1300	-	280	-	ns
SCL clock high period	$t_{(HIGH)}$	4000	-	600	-	60	-	ns
Data rise time	t_{RD}		1000		300		120	ns
Data fall time	t_{FD}	-	300	-	300	-	150	ns
Clock rise time	t_{RC}	-	1000	-	300	-	40	ns
Clock fall time	t_{FC}	-	300	-	300	-	40	ns

Notes:

- A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{(HDDAT)}$ has only to be met if the device does not stretch the LOW period ($t_{(LOW)}$) of the SCL signal.
- A Fast-mode I²C-bus device can be used in a Standard-mode I²C -bus system, but the requirement $t_{(SUDAT)}$ >250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.

If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{(SUDAT)}$ = 1000 + 250 = 1250ns (according to the Standard-mode I²C -bus specification) before the SCL line is released.

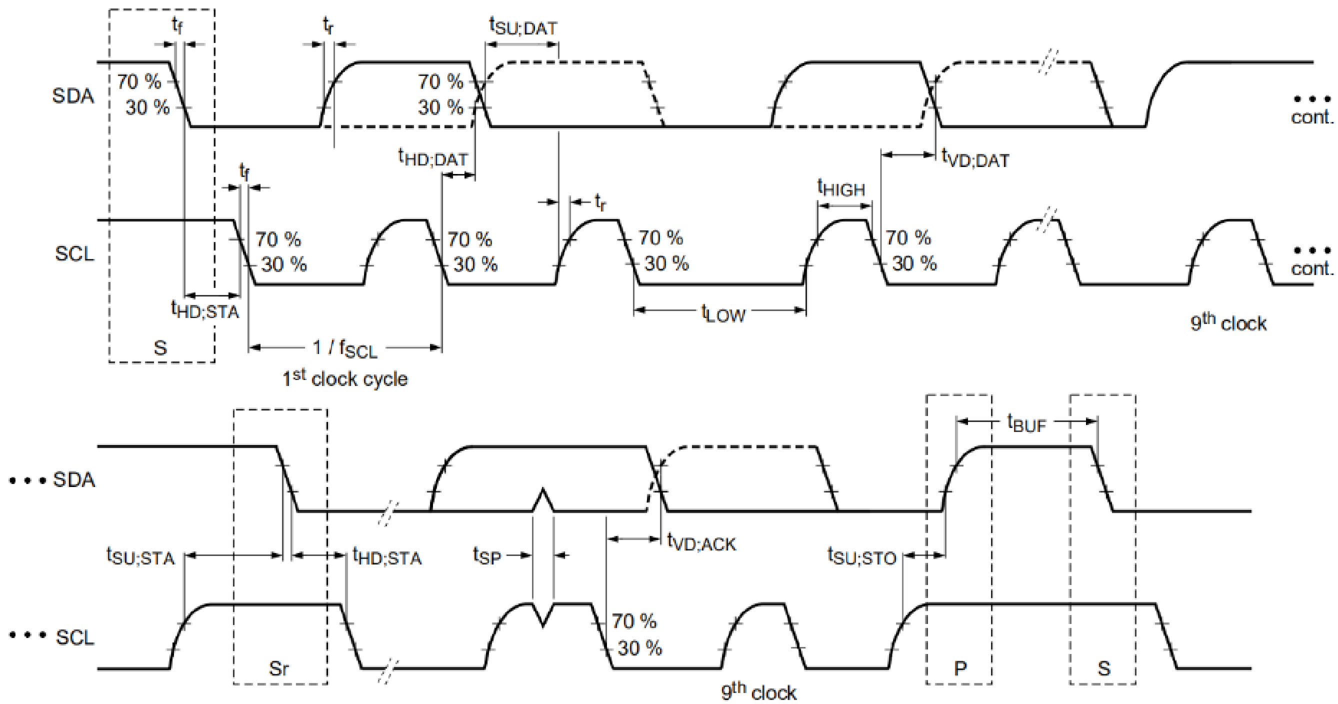


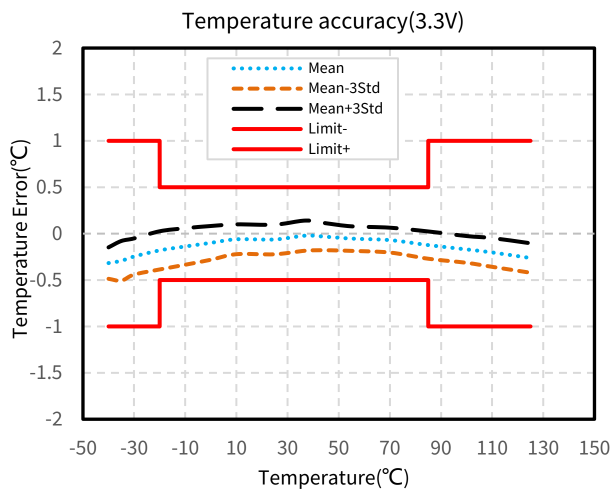
Figure 2.1 I²C Timing Diagram

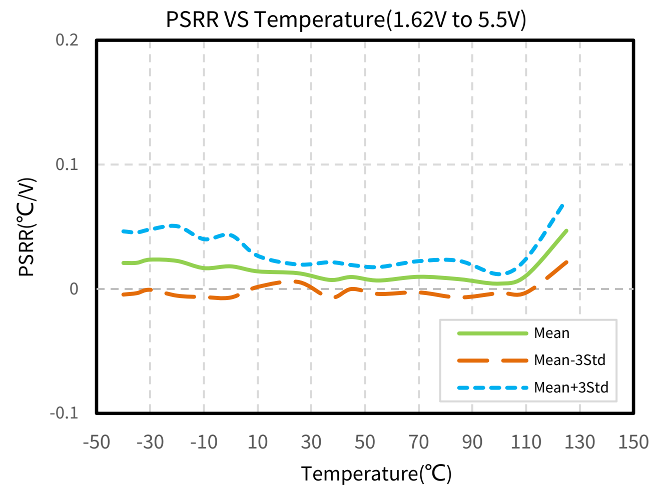
2.5. Thermal Information

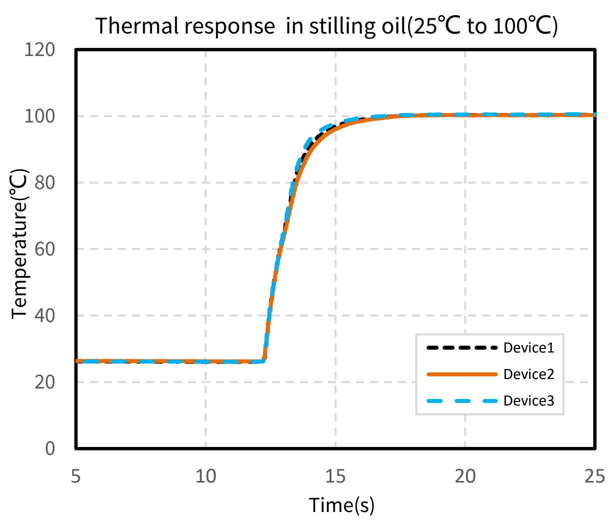
Thermal Metric		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.2	°C/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	67.4	°C/W
φ_{JT}	Junction-to-top characterization parameter	15	°C/W
φ_{JB}	Junction-to-board characterization parameter	79	°C/W

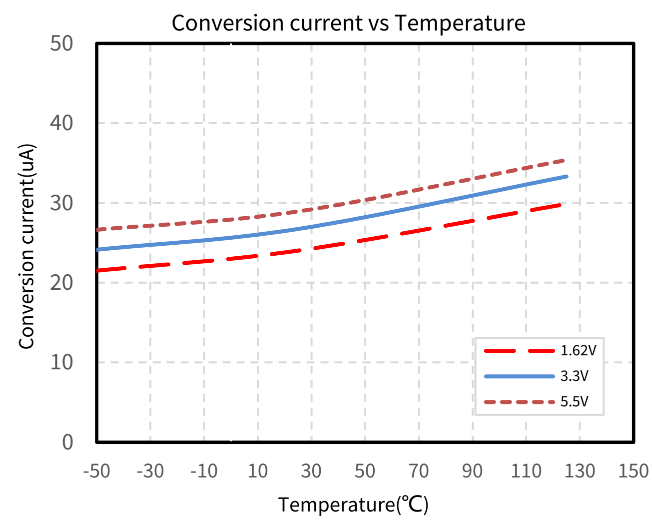
2.6. Typical Characteristics

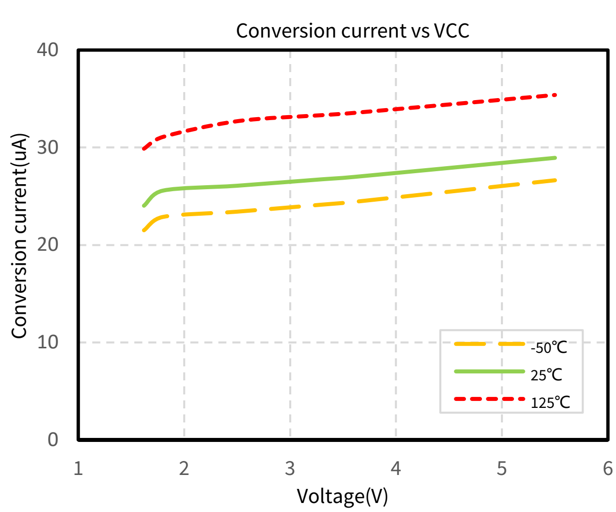
at TA = +25°C and VDD = 3.3 V, Rpu = 5.1kohm, unless otherwise noted.











3. Function Description

3.1. Overview

The Digital temperature sensor NST175-Q1 has a wide supply voltage range of 1.62V to 5.5V. The NST175-Q1 measures temperature using a band-gap structure and 12-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). In the range of –20°C to 85°C, the typical accuracy is ±0.2°C, and in the range of –40°C to 125°C the maximum accuracy is ±1°C.

The NST175-Q1 communicates with the master device through a 2-wire interface (SMBus and I^2C), which operates up to 400kHz in I^2C fast mode and 2MHz in I^2C High speed mode. On the same 2-wire bus, the NST175-Q1 allows up to 27 devices, by three address pins. The NST175-Q1 has a bus fault timeout feature, if the SDA line remains low for more than $T_{TIMEOUT}$ (see specification), it will reset to the IDLE state (SDA set to high impedance) and wait for a new start condition, and it should be noted that when in Shutdown Mode, the TIMEOUT feature is not functional. An integrated low-pass filter on both the SDA and the SCL line of the NST175-Q1, its communications are reliable in noisy environments by these filters.

3.2. Functional Block Diagram

The NST175-Q1 Functional Block Diagram as shown in Figure 3.1.

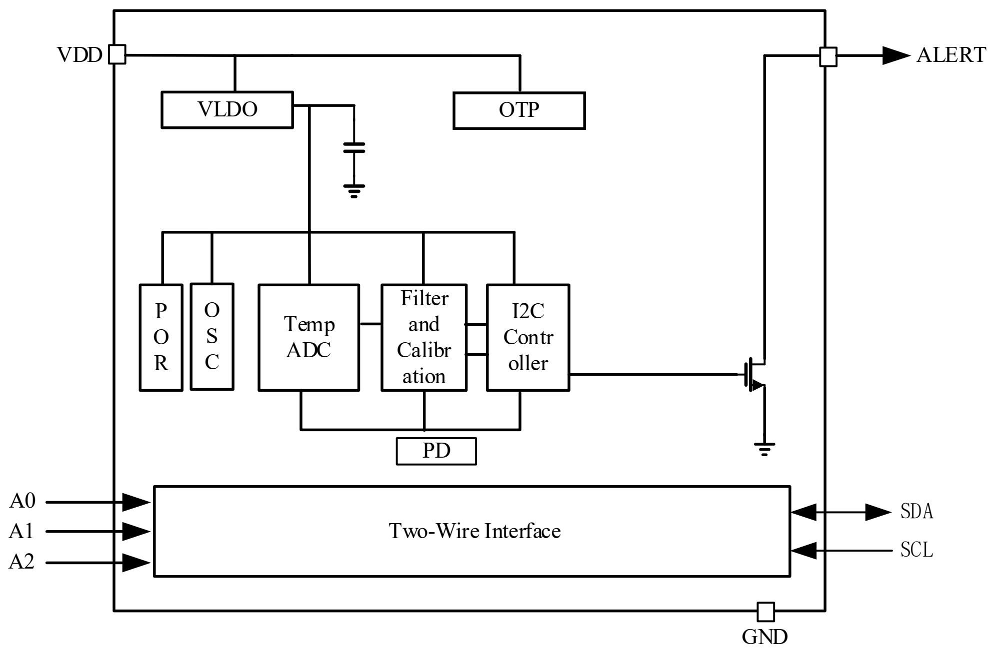


Figure 3.1 NST175-Q1 Functional Block Diagram

3.3. Device Functions

3.3.1. Shutdown Mode (SD)

For power-sensitive applications, The NST175-Q1 device offers a low-power shutdown mode, which reducing current consumption to typically less than 0.1 µA. Shutdown mode is enabled when write 1 to SD bit of the configuration register. In shutdown mode a One-shot command can be sent to perform a temperature transition, and the device shuts down automatically when the temperature transition is complete. When SD write to 0, the device maintains a continuous conversion state. For the NST175-Q1, Time-out feature is turned off in Shutdown Mode.

3.3.2. One-shot (OS)

The NST175-Q1 supports a one-shot temperature measurement mode when continuous temperature monitoring is not required. First set the chip into shutdown mode, write 1 to the OS bit to wake up the chip once and perform a temperature conversion. During the conversion, the OS bit reads 0. After the single conversion is complete, the device returns to the Shutdown state. At the end of the conversion, the OS bit reads 1.

3.3.3. Converter Resolution

The converter resolution bits control the resolution of the internal ADC. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. The resolution bits and the relationship between resolution and conversion time, please refer to Congfiguration Register.

3.3.4. Temperature Alert

NST175-Q1 also incorporates a digital comparator that compares a series of readings (the number of which can be selected by the user) with user-programmable setpoint. The comparator triggers the ALERT pin state, which is programmable for mode and polarity. allowing the user to define the number of consecutive error conditions that must occur before ALERT is activated.

3.3.5. Thermostat Mode (TM)

The thermostat mode bit of the NST175-Q1 indicates whether the device is operating in Comparator mode (TM = 0) or interrupt mode (TM = 1).

Comparator Mode (TM = 0): In comparator mode (TM = 0), when the temperature is equal to or exceeds the value of the $\mathbf{T_{HIGH}}$ register, the alert pin is activated until the temperature is lower than the value of the $\mathbf{T_{LOW}}$ register.

Interrupt Mode (TM = 1): In interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds $\mathbf{T_{HIGH}}$ or goes below $\mathbf{T_{LOW}}$ registers. When the main controller reads the temperature register, the alert pin is cleared. For more information about comparison mode and interrupt mode, see the *High and Low Limit Registers* section.

3.3.6. Polarity

The polarity bit allows the user to control the output polarity of the NST175-Q1 AL bit. When POL bit is 0, AL bit is active low, when POL bit is 1, AL bit is active high, while the state of AL bit is inverted. And the operation of AL bit in different modes is shown in Figure 3.2.

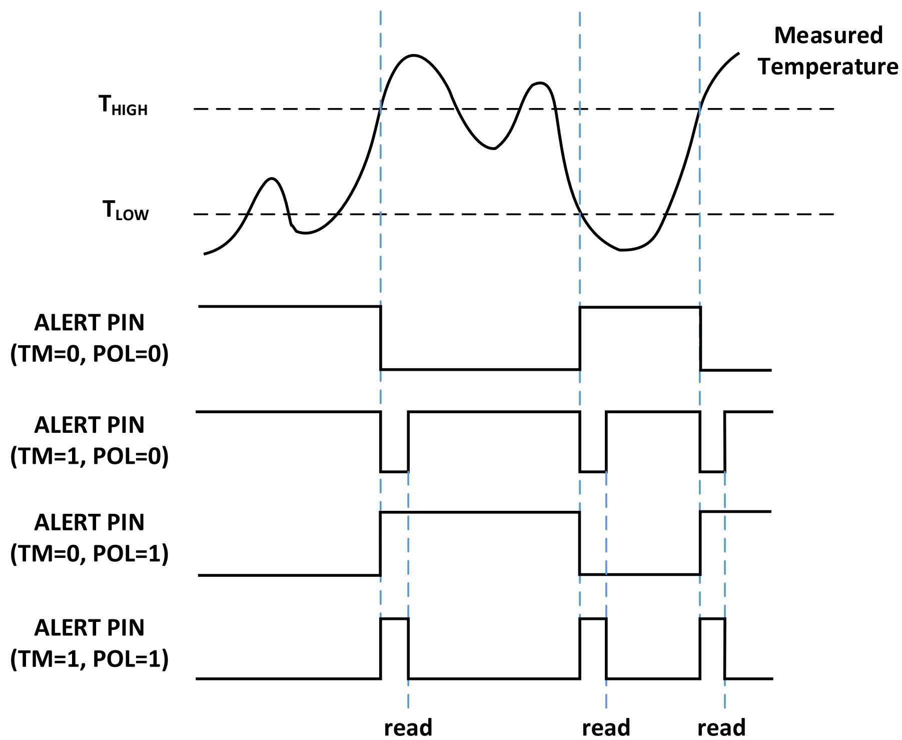


Figure 3.2 Output Transfer Function Diagram

3.3.7. Fault Queue

A fault condition is generated when the temperature measurement value exceeds the T_{HIGH} and T_{LOW} register values, and the number of fault conditions activated by the trigger alert can be programmed by the fault queue. False triggering of alerts due to temperature noise can be avoided by using a fault queue. The number of measured faults that can be programmed to trigger a device alert condition, please refer to Congfiguration Register. See the *High and Low Limit Registers* section for the format and byte order of the T_{HIGH} and T_{LOW} registers.

3.4. Serial Bus

The NST175-Q1 is compatible with SMBus and I²C interfaces. data on the I²C-bus can be transferred at rates of up to 100kbit/s in the Standard-mode, up to 400kbit/s in the Fast-mode, or up to 2Mbit/s in the High-speed mode. All data bytes are transmitted MSB-firstly.

3.4.1. Bus Overview

The device on the bus that initiates the transmission is referred to as the master device, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls bus access and generates START and STOP conditions.

3.4.2. Bus Address

For communication between the master and the slave, a byte address needs to be sent first, including 7bit slave address bits and 1bit read and write direction bits. NST175-Q1 has three address pins, allowing up to 27 devices to be addressed on one bus interface. Table 3.1 describes the pin logic levels used to properly connect up to 27 devices. “1” indicates the pin is connected to the supply (VDD); “0” indicates the pin is connected to GND; “float” indicates the pin is left unconnected. The state of pins A0, A1, and A2 is sampled on every bus communication and must be set prior to any activity on the interface.

Table 3.1 Address Pins and Slave Addresses for the NST175-Q1

A0	*A1*	*A2*	*SLAVE ADDRESS*	
			BINARY	*HEX*
0	0	0	1001000	48
1	0	0	1001001	49
0	1	0	1001010	4A
1	1	0	1001011	4B
0	0	1	1001100	4C
1	0	1	1001101	4D
0	1	1	1001110	4E
1	1	1	1001111	4F
0	0	Float	1110000	70
Float	0	Float	1110001	71
1	0	Float	1110010	72
0	1	Float	1110011	73
Float	1	Float	1110100	74
1	1	Float	1110101	75
0	Float	Float	1110110	76
1	Float	Float	1110111	77
0	Float	0	0101000	28
1	Float	0	0101001	29
0	Float	1	0101010	2A
1	Float	1	0101011	2B
Float	0	0	0101100	2C
Float	1	0	0101101	2D
Float	0	1	0101110	2E
Float	1	1	0101111	2F
Float	Float	0	0110101	35
Float	Float	1	0110110	36
Float	Float	Float	0110111	37

3.4.3. Bus Function

- **Writing and Reading**

Writing operation is triggered by sending the slave address in write mode (R/W=0), then the master sends pointer register, and send the data byte afterwards. The transaction is ended by a STOP condition.

During writing operation, NST175-Q1 is used as the slave receiver. The master transfers the slave address byte firstly, including 7 address bits and 1bit write direction bits, NST175-Q1 acknowledges after receiving the valid address. the second byte transmitted by master is the pointer register address, then NST175-Q1 acknowledges and the next byte of data is written to the pointer register. The master can terminate communication by generating a STOP condition. The details of this sequence are shown in Figure 3.4.

To be able to read registers, firstly the register address must be sent in write mode (R/W=0), then either a stop or a repeated start condition must be generated. When the slave is addressed as read mode (R/W=1), then the slave sends out 1 byte data. After reading the data the master needs to generate the NACK and stop condition to end the transaction. The details of this sequence are shown in Figure 3.5.

If repeated reads from the same register are required, it is not necessary to send the pointer register byte repeatedly because the NST175-Q1 remembers the pointer register value until it is changed by the next write operation.

- **SMBus Alert Function**

When the NST175-Q1 is operating in interrupt mode (TM=1), the NST175-Q1 supports the SMBus Alert function, the ALERT pin of the NST175-Q1 can be connected as a SMBus Alert signal. When the master monitors that the alert is active, the master can send the SMBus alert command (00011001) on the bus, if the ALERT pin of the NST175-Q1 is active, the device responds to the SMBus Alert command by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether a temperature above T_{HIGH} or below T_{LOW} has caused an ALERT condition: this bit is high if the temperature is greater than or equal to T_{HIGH}. the bit is low if the temperature is less than T_{LOW}. The details of this sequence are shown in Figure 3.6.

If multiple slaves respond to the SMBus alert command issued by the master, the SMBus alert arbiter will arbitrate to determine which slave to clear the alert status. The one with the lowest slave address wins the arbitration. If the NST175-Q1 wins the arbitration, the ALERT pin of the NST175-Q1 is cleared when the SMBus ALERT command is completed. If NST175-Q1 loses arbitration, the ALERT pin of NST175-Q1 will not be cleared.

- **General Call**

The NST175-Q1 provides the general call function. when the general call address (0 000 000) sent by host is received and the R/W bit is 0, the device replies to the command. If the second byte is 00000110, the NST175-Q1 latches the state of its address pins and resets its internal registers to the value at power-up.

- **High-Speed Mode**

The NST175-Q1 supports bus operation above 400 kHz, requiring that the master device must switch the bus to high-speed mode operation by issuing a high-speed mode master code (00001XXX) in the first byte after the START condition. The NST175-Q1 does not acknowledge this byte, the NST175-Q1 switches the input filter of SCL, SDA and output filter of SDA to high-speed mode, allowing data transfer up to 2MHz(For VDD<1.8V, the Hs-mode up to 1.6MHz). After issuing the master code for high-speed mode, the master will transmit a two-wire slave address to initiate the data transfer operation. The bus will continue to operate in high-speed mode until a stop signal appears on the bus. Once the stop signal is received, the SCL, SDA input filter and SDA output filter of the NST175-Q1 switch to the fast mode.

- **Time-out Function**

The NST175-Q1 resets the I²C interface when the SCL or SDA is continuously pulled low for 54ms (typical) between the START and STOP signals, the NST175-Q1 release the SDA and SCL line and waits for the master to initiate a START condition. To avoid activating the timeout function, the SCL operating frequency must be maintained at a rate of at least 1kHz.

- **I²C Timing**

The NST175-Q1 devices supports SMBus and I²C interfaces. Figure 3.3 to Figure 3.6 describe the various Bus operations on the NST175-Q1. The following list provides bus definitions. Parameters for Figure 3.3 are defined in the I²C Timing Requirements.

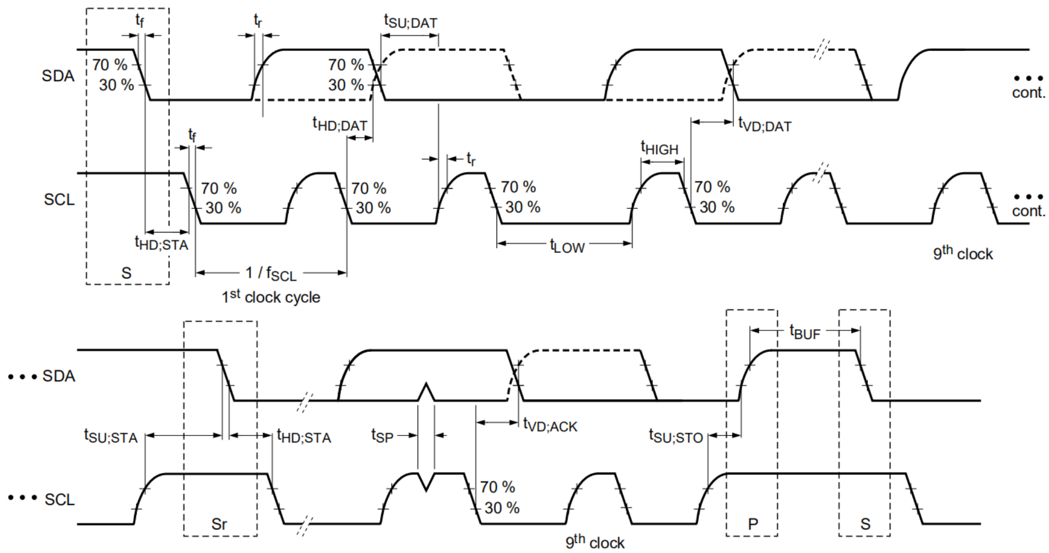


Figure 3.3 I²C Timing Diagram

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A high-to-low transition of SDA with SCL high is a START condition which must precede any other command.

Stop Data Transfer: A low-to-high transition of SDA with SCL high is a STOP condition. The termination of each data transfer can be done with a RESTART or STOP.

Data Transfer: The amount of data bytes transferred between START and STOP is controlled by the master and is unlimited. The receiver acknowledges the transfer of data.

Acknowledge: All addresses and data words are serially transmitted to and from the device in 8-bit words. The device sends a zero to acknowledge that it has received each word when the address is matched. This happens during the ninth clock cycle. The data transfer can be terminated by the host generating a not-acknowledge during the host receiving data.

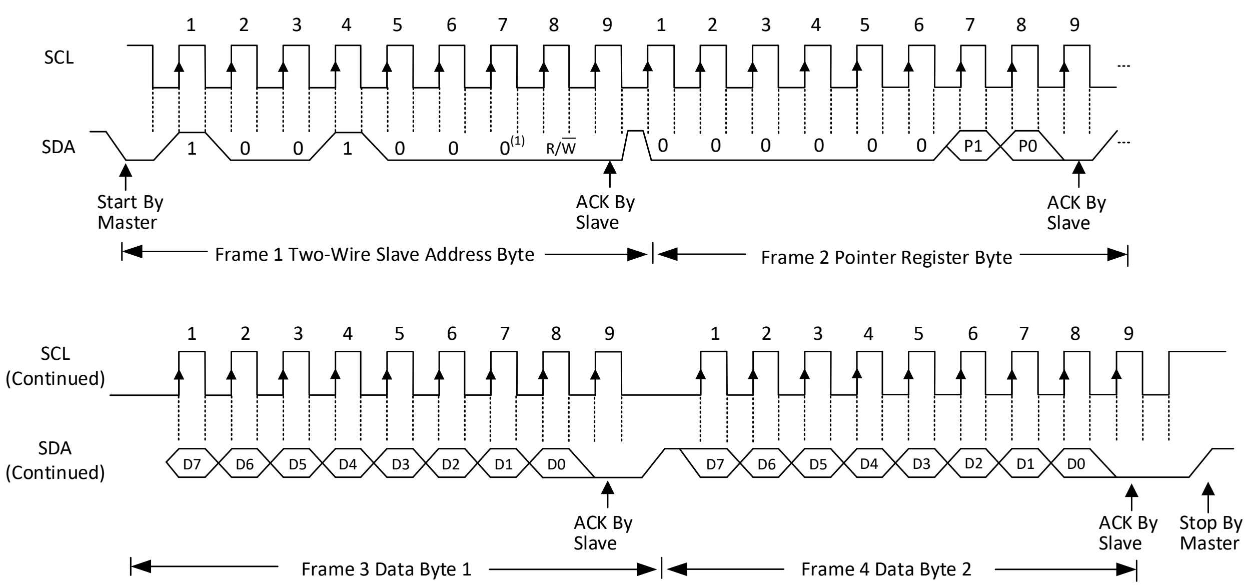


Figure 3.4 I²C Timing Diagram for the NST175-Q1 Write Word Format

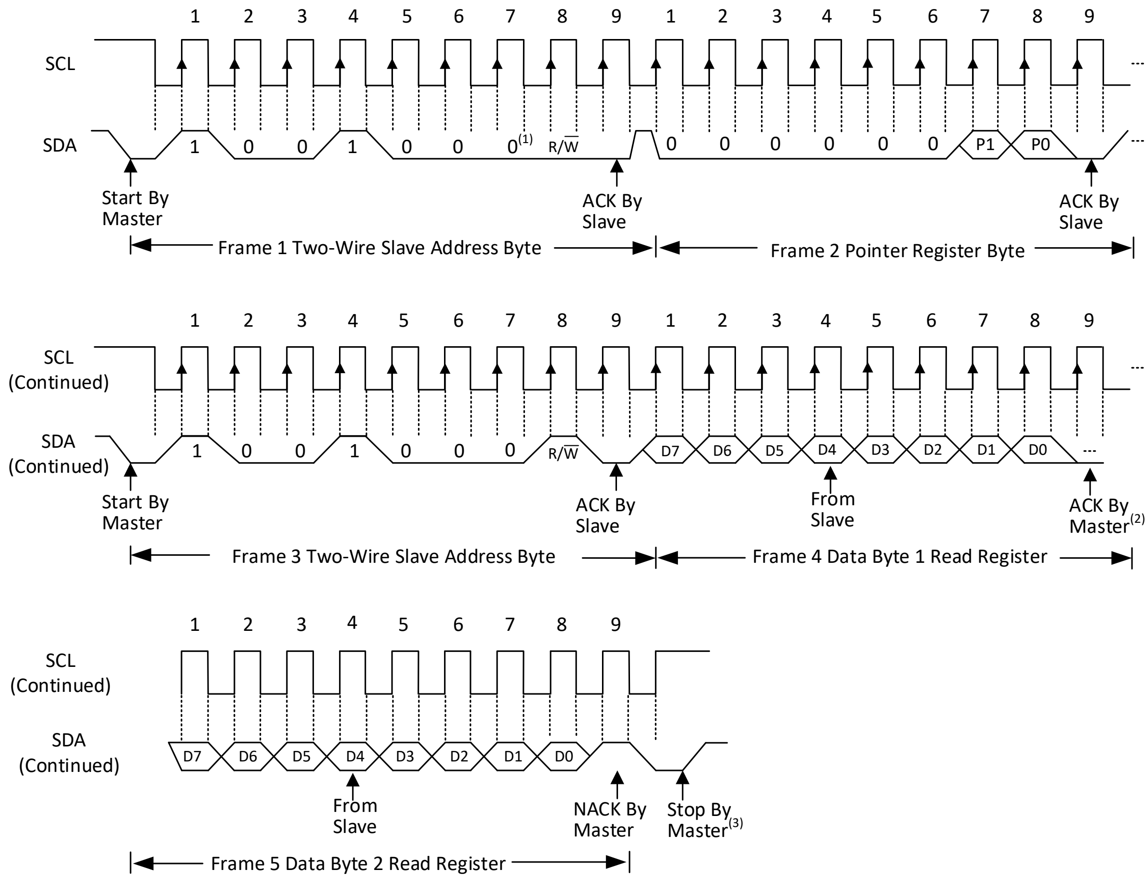


Figure 3.5 I²C Timing Diagram for Read Word Format

(1) Slave address 1001000 is shown.
(2) Master should leave SDA high to terminate a single-byte read operation.
(3) Master should leave SDA high to terminate a two-byte read operation.

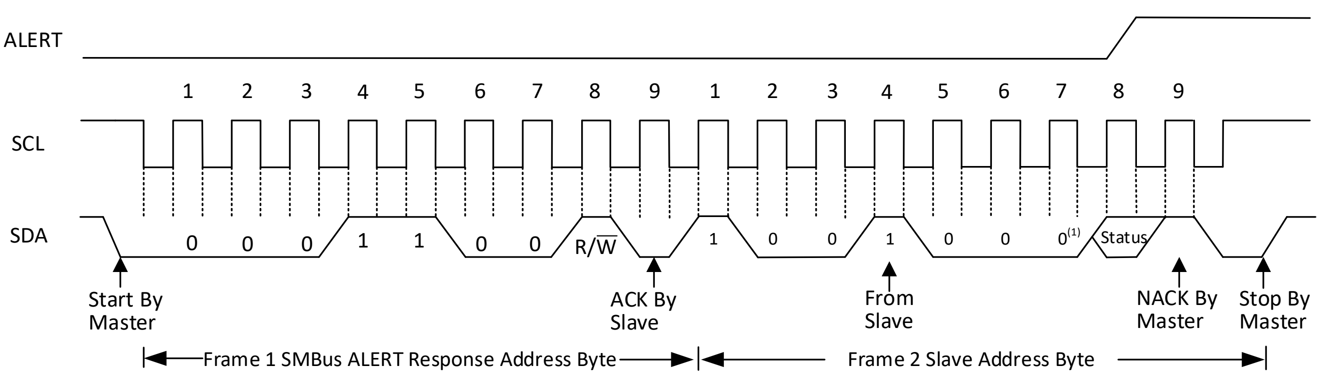


Figure 3.6 Timing Diagram for SMBus ALERT

4. On-Chip Register

4.1. Pointer Register

Figure 4.1 shows the internal register structure of the NST175-Q1. The 8-bit Pointer register of the devices is used to address a given data registers. The Pointer register uses the two LSBs to identify which of the data registers must respond to a read or write command. Table 4.1 identifies the bits of the Pointer Register Byte. Table 4.2 describes the Pointer Address of the Registers available in the NST175-Q1. Power-up reset value of P2/P1/P0 is 000.

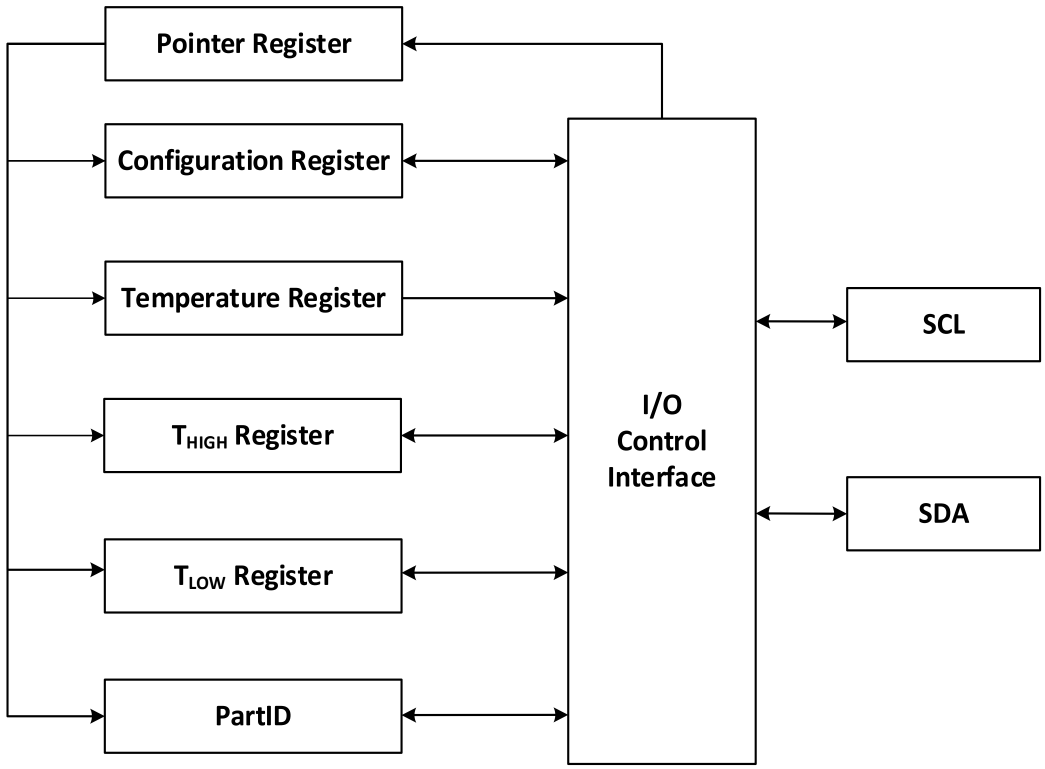


Figure 4.1 Internal Register Structure of the NST175-Q1

Table 4.1 Pointer Register Byte

P7	*P6*	*P5*	*P4*	*P3*	*P2*	*P1*	*P0*
0	0	0	0	0	Register bit		

Table 4.2 Pointer Register Description

BIT NO.	*Name*	*Description*
Bits 7:3	**NA**	P3 to P7 must always be 0 during the write command.
Bits 2:0	**Pointer[2:0]**	**000:** Temperature register (default) **001:** Configuration register **010:** T_{LOW} register **011:** T_{HIGH} register **111:** PartID register

4.2. Temperature Register

The temperature register is a read-only register used to store the results of each completed temperature conversion, which consists of 2 Bytes in the format shown in Table 4.3 , with MSB output first and followed by the LSB, and 12-bit MSBs used to indicate the temperature value.The data format for temperature is listed in Table 4.4, the resolution is 0.0625°C. Negative numbers are represented in binary complement format. After power-up or reset and before the first temperature conversion is completed, the value of the temperature register is 0.

By addressing the Configuration register and setting the resolution bits accordingly. The user can obtain 9, 10, 11, or 12 bits of resolution. For 9, 10, 11, or 12-bit resolution, the unused least significant bits (LSBs) set to 0.

Table 4.3 Temperature Register(12-bit)

Bit	***D15***	***D14***	***D13***	***D12***	***D11***	***D10***	***D9***	***D8***
Name	T11	T10	T9	T8	T7	T6	T5	T4
R/W	R	R	R	R	R	R	R	R
Bit	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***
Name	T3	T2	T1	T0	-	-	-	-
R/W -	R	R	R	R	R	R	R	R

Table 4.4 Temperature Data Format(12-bit)

TEMPERATURE(°C)	***DIGITAL OUTPUT***	
	BINARY	***HEX***
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-40	1101 1000 0000	D80

4.3. Configuration Register

The Configuration register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the NST175-Q1 is shown in Table 4.5, followed by a breakdown of the register bits, as shown in Table 4.6. The power-up or reset value of the Configuration register are all bits equal to 0.

Table 4.5 Configuration Register Format

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OS	R1	R0	F1	F0	POL	TM	SD
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4.6 Configuration Register Description

Bit No.	Name	Description
Bit 7	**OS**	**0:** Continuous-Conversion Mode (default) **1:** One-shot Mode
Bits 6:5	**Converter Resolution [1:0]**	**00:** 9bit (0.5°C default) **01:** 10bit (0.25°C) **10:** 11bit (0.125°C) **11:** 12bit (0.0625°C)
Bits 4:3	**Fault Queue [1:0]**	**00:** Consecutive faults are 1 (default) **01:** Consecutive faults are 2 **10:** Consecutive faults are 4 **11:** Consecutive faults are 6
Bit 2	**Polarity**	**0:** AL bit is active low (default) **1:** AL bit is active High
Bit 1	**Thermostat**	**0:** Comparator mode (default) **1:** Interrupt mode
Bit 0	**Shutdown**	**0:** Continuous-Conversion Mode (default) **1:** Shutdown Mode

4.4. High and Low Limit Registers

In comparator mode (TM = 0), the ALERT pin of the NST175-Q1 becomes active when the temperature equals or exceeds the value in THIGH and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When the ALERT pin is cleared, it only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the general call reset command. This action also clears the state of the internal registers in the device by returning the device to comparator mode (TM = 0).

Table 4.7 and Table 4.8 describe the format for the T_{HIGH} and T_{LOW} registers. The most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are: THIGH = 80°C and TLOW = 75°C

The format of the data for THIGH and TLOW is the same as for the Temperature register.

Table 4.7 T_{LOW} Register (02H) (12-bit)

Bit	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Name	H11	H10	H9	H8	H7	H6	H5	H4
Default	0	1	0	0	1	0	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	H3	H2	H1	H0	-	-	-	-
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4.8 T_{HIGH} Register (03H) (12-bit)

Bit	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Name	H11	H10	H9	H8	H7	H6	H5	H4
Default	0	1	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	H3	H2	H1	H0	-	-	-	-
Default	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

All 12 bits for the Temperature, THIGH, and TLOW registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in THIGH and TLOW can affect the ALERT output even if the converter is configured for 9-bit resolution.

4.5. Product ID Register

Table 4.9 Product ID Register

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Default	1	0	1	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R

D4--D7: Product Identification Nibble. Always returns **Ah** to uniquely identify this part as the NST175-Q1.

D0--D3: Die Revision Nibble. Returns **1h** to uniquely identify the revision level as one.

5. Application

5.1. Typical Application

No external components are required to operate the NST175-Q1 other than pull-up resistors on SCL, SDA and ALERT, a bypass capacitor of 0.01µF is recommended. the sensing device for the NST175-Q1 device is the device itself. The thermal path is through the package leads as well as the plastic package. The low thermal resistance of the metal results in the leads providing the primary thermal path. The typical application of NST175-Q1 is shown in Figure 5.1.

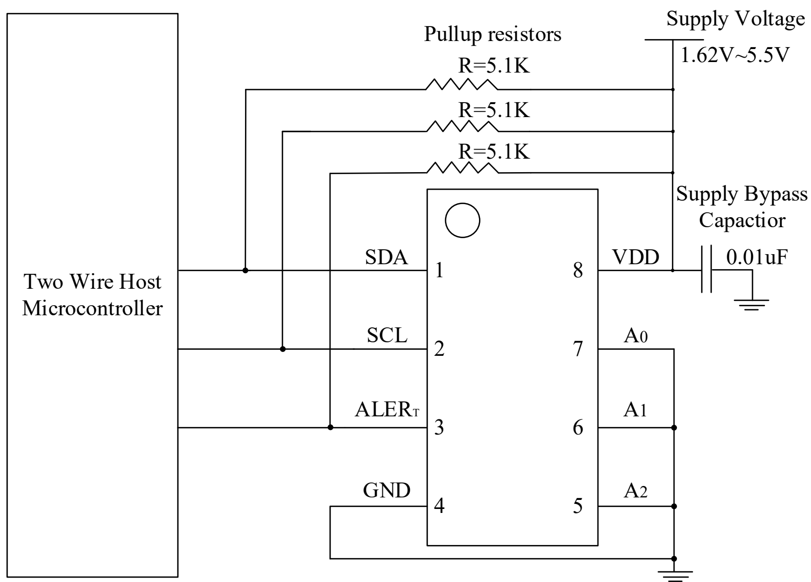
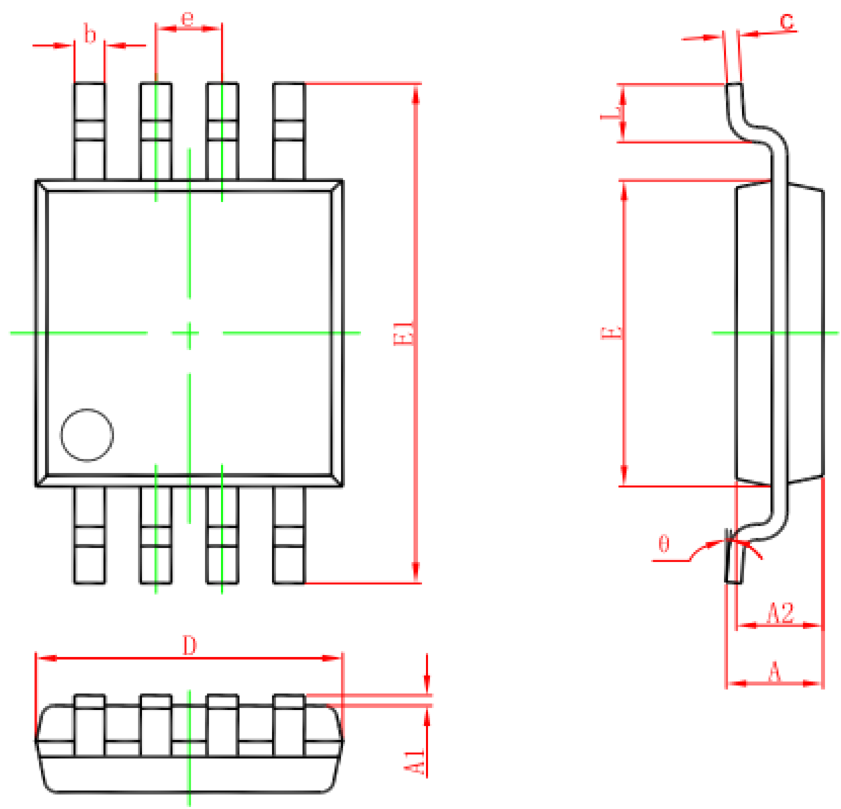


Figure 5.1 Typical Connections of NST175-Q1

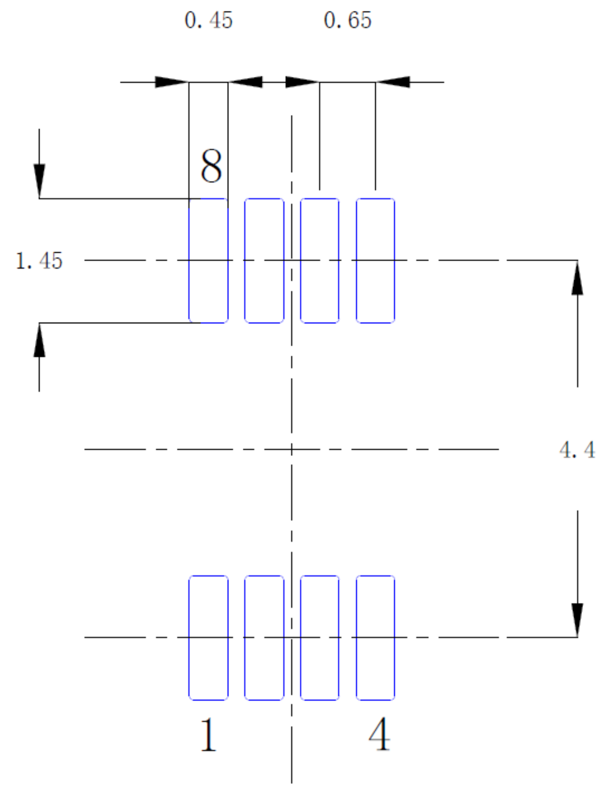
6. Package Information

6.1. Package

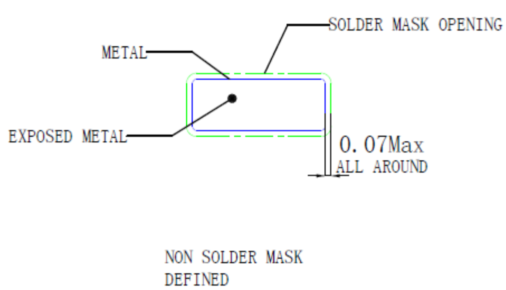
6.1.1. MSOP (8) Package

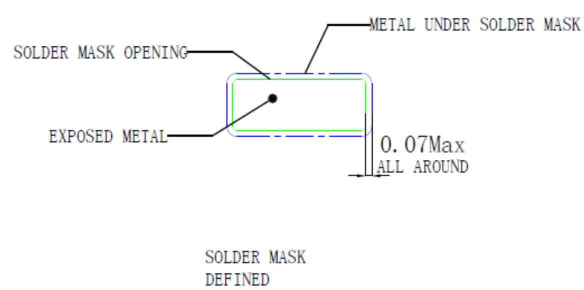


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0. 820	1. 100	0. 032	0. 043
A1	0. 020	0. 150	0. 001	0. 006
A2	0. 750	0. 950	0. 030	0. 037
b	0. 250	0. 380	0. 010	0. 015
c	0. 090	0. 230	0. 004	0. 009
D	2. 900	3. 100	0. 114	0. 122
e	0.650(BSC)		0.026(BSC)	
E	2. 900	3. 100	0. 114	0. 122
E1	4. 750	5. 050	0. 187	0. 199
L	0. 400	0. 800	0. 016	0. 031
θ	0°	6°	0°	6°



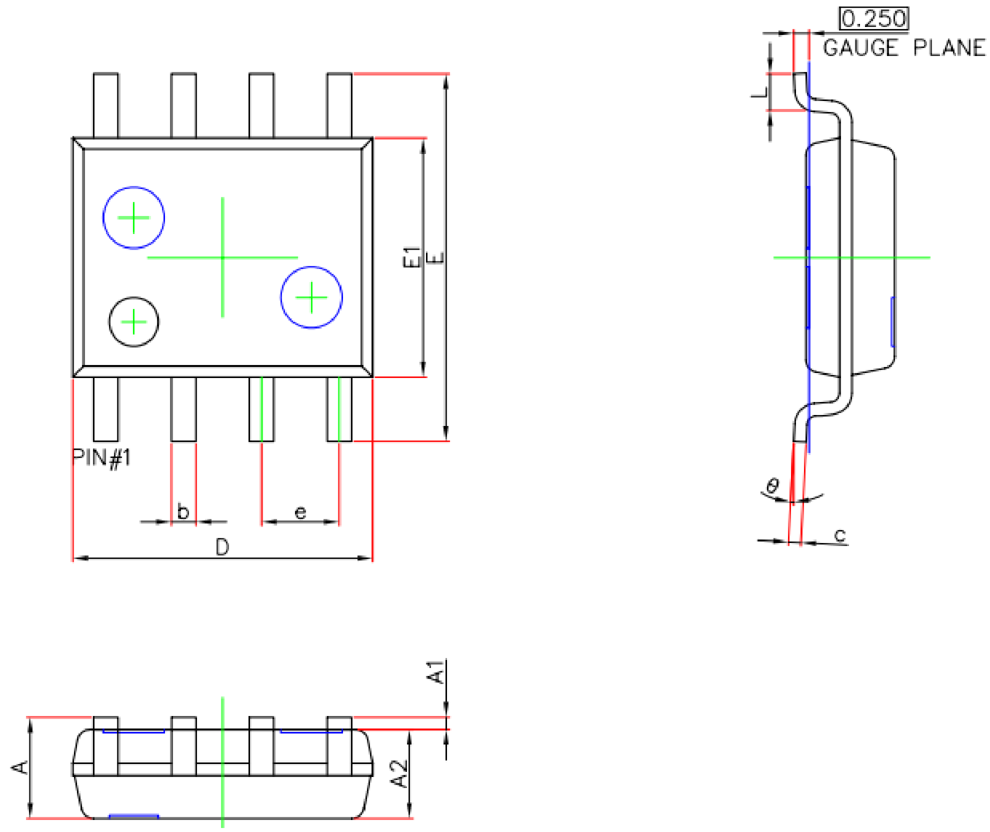
LAND PATTERN EXAMPLE



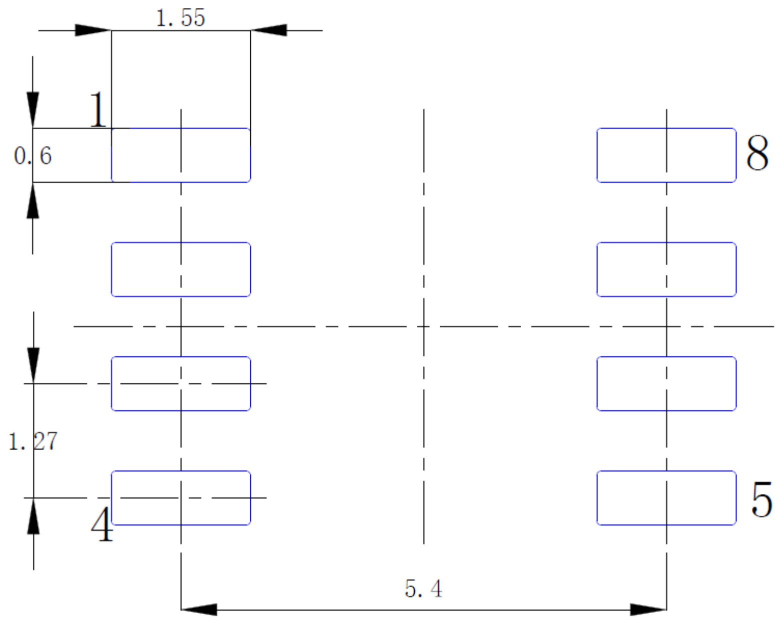


Note: All Linear dimensions are in millimeters.

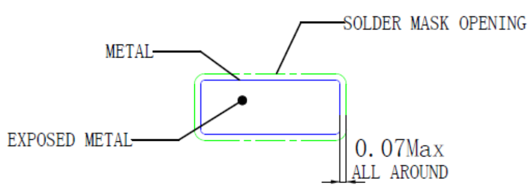
6.1.2. SOP (8) Package



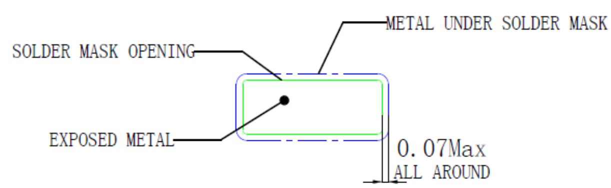
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



LAND PATTERN EXAMPLE



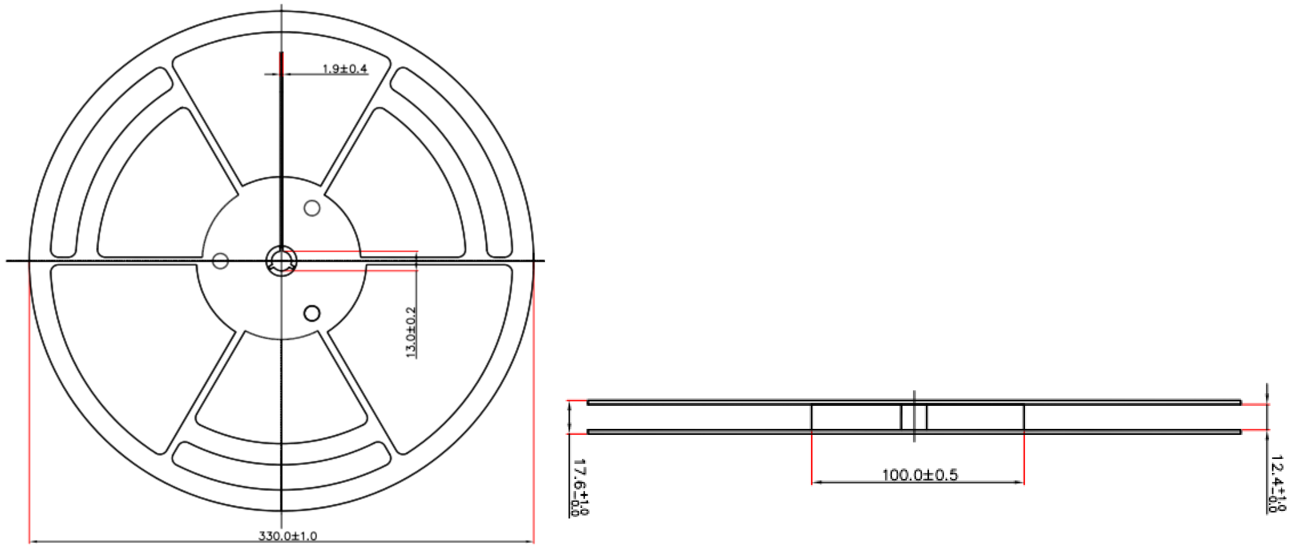
NON SOLDER MASK DEFINED



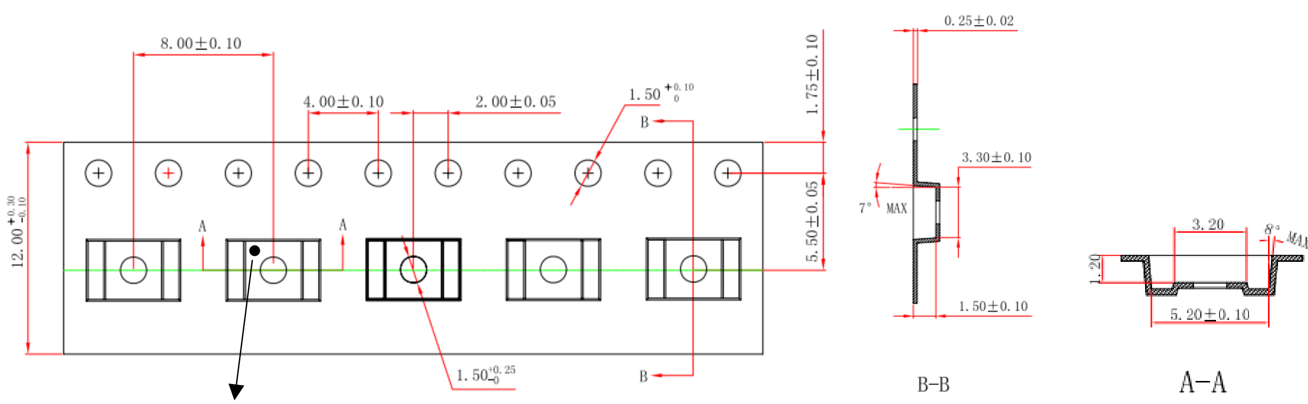
SOLDER MASK DEFINED

Note: All Linear dimensions are in millimeters.

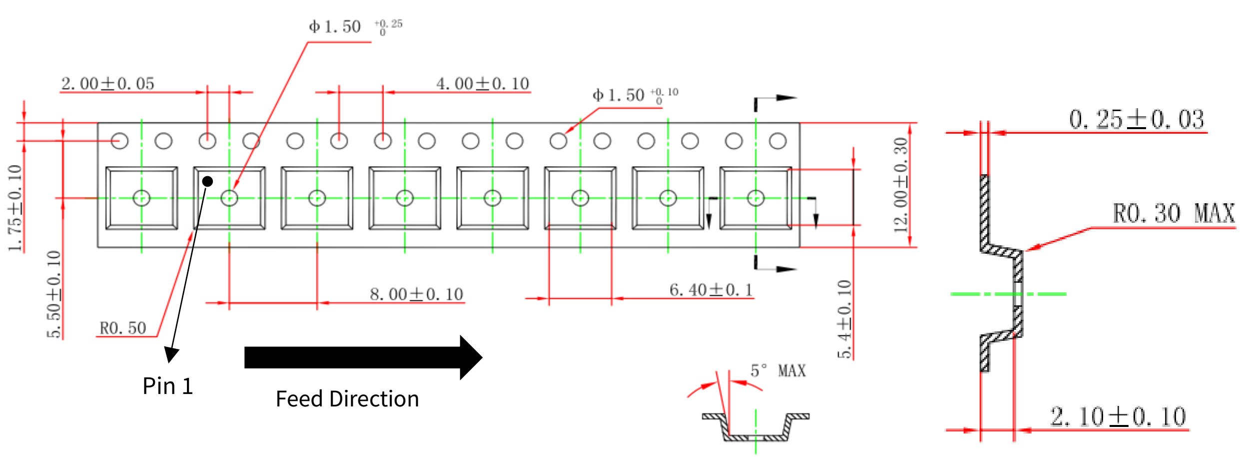
6.2. Tape and Reel Information



REEL Information (in mm)



MSOP (8) TAPE Information (in mm)



SOP (8) TAPE Information (in mm)

7. Order Information

Type	Unit	MSL	Marking	Description
NST175H-Q1MSR	4000ea/Reel	1	186H XXXQXX	MSOP (8) package, Reel
NST175H-Q1SPR	4000ea/Reel	1	NST 175HQ XXXXXX	SOP (8) package, Reel
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260°C according to the JEDEC industry standard classifications and peak solder temperatures (Reflow profile: J-STD-020E).				

8. Marking Information

Type	Line	Name	Remark
186H XXXQXX	Line1	186H	Fixed product code
	Line2	XXXQXX	Tracking code
NST 175HQ XXXXXX	Line1	NST	Fixed product code
	Line2	175HQ	
	Line3	XXXXXX	Tracking code

9. Revision History

Revision	***Description***	***Date***
0.1	Initial Version	2024/3/22
1.0	Mp Version	2024/7/31

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