NOVOSENSE

NSD8306-Q1, NSD8306A-Q1

Multi-channel Half Bridge Driver

Datasheet (EN) 1.4

Product Overview

The NSD8306/NSD8306A is a multi-channel half-bridge driver for automotive applications including HVAC flap DC motors, side mirror adjustment / fold motors, general relays, or other LEDs.

With the different connection configuration of half-bridge power stage outputs, the device can driver DC motors in simultaneous, sequential, or parallel mode. The outputs also support DC motor in forward, reverse, slow decay, and fast decay operation.

The device includes 6x internal configurable PWM generators, which allow for flexible control for LED dimming or motor current limitation during start up or stall condition.

The integrated serial peripheral interface (SPI) controls all outputs and provides diagnostic information including normal operation, POR, VM undervoltage/overvoltage, overcurrent, over temperature protection and open load status.

The device features sleep mode with low quiescent current when EN input is low or VDD falls below POR threshold.

Applications

- HVAC DC motors
- Side mirror adjustment and mirror fold
- Relays
- LEDs

Device Information

Part Number	Package	Body Size
NSD8306-Q1HTSXR	HTSSOP24	7.80mm × 4.40mm
NSD8306A-Q1HTSBR	HTSOP24	8.65mm × 3.90mm

Key Features

- 6x half bridge driver
  - 1A per HB channel, 3A max for all channel all on
  - Half bridge output can be in parallel
- AEC-Q100 Grade1 Qualified
- Wide 4.5V to 36V (configurable) operating Voltage
- Very low quiescent sleep mode
- PWM mode with internal PWM generation on each channel
  - 4 PWM frequency options: 80/100/200/2000 Hz
  - Duty cycle 8-bit resolution (1/255, ~0.4 % duty)
- Integrated diagnosis and fault protection features
  - VM undervoltage & overvoltage protection (UV&OV)
  - Overcurrent / short circuit Protection (OCP/SCP)
  - Over temperature warning & shutdown
  - Open load diagnosis
  - Dedicated nFault indicator pin
- HB output Slew rate control two options:

  0.6V/μs(default) / 2.5V/μs
- HTSSOP24, 7.8mm X 4.4mm with exposed pad option
- HTSOP24, 8.65mm x 3.9mm with exposed pad option
- RoHS& REACH Compliance

Functional Block Diagrams

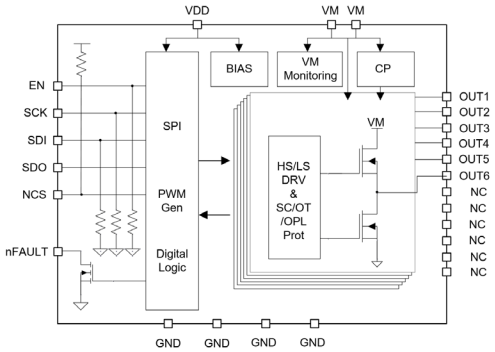

Figure 1. NSD8306/NSD8306A Block Diagram

1. Pin Configuration and Functions

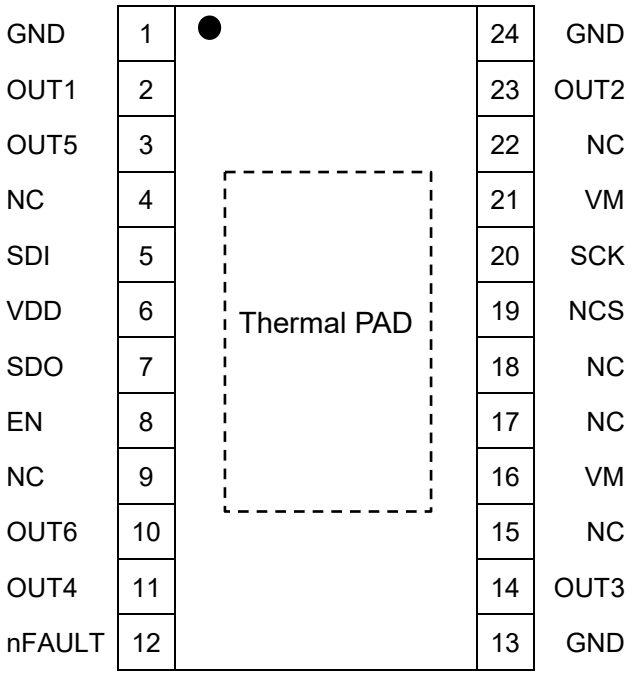

Figure 2. NSD8306/NSD8306A Pinout

Table 1.1 NSD8306/NSD8306A Pin Description

Symbol	*NO.*	*Type*	*Description*
GND[1]	1,13, 24	PWR	Pins for ground connection, all ground pins should be externally connected together.
OUT1	2	O	Half-bridge output1 pin.
OUT5	3	O	Half-bridge output5 pin.
SDI	5	I	SPI data input pin
VDD	6	PWR	Logic supply input pin,
SDO	7	O	SPI data output pin
EN	8	I	Driver enable input pin with internal pull down (active HIGH). If EN input pin is pulled low, all OUTx go to tri-state and device move to low-power sleep state.
NC	4,9,15, 17,18,22	-	Not connected
OUT6	10	O	Half-bridge output6 pin.
OUT4	11	O	Half-bridge output4 pin.

nFAULT	12	O	Fault alert indicator output (active LOW). Open drain structure requires external pull up resistor, typical 4.7Kohm can be used.
OUT3	14	O	Half-bridge output3 pin.
VM	16,21	PWR	5V to 36V power supply. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient bulk capacitor (>10uF) needs to guarantee VM pin voltage in maximum range. Put the 0.1uF and bulk capacitor (>10uF) close to the VM pin. Two VM pins should be externally connected together.
NCS	19	I	SPI chip select input pin.
SCK	20	I	SPI clock input pin.
OUT2	23	O	Half-bridge output2 pin.
Thermal PAD[1]	—		Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

Note:

1. When using the NSD8306A (only HTSOP24 package), pin 13 & pin 24 can optionally be left floating, and in this case, the bottom thermal pad must have a reliable connection to the ground plane (GND).

2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VM	Power supply voltage	–0.3	40	V
VDD	Logic supply voltage	–0.3	6	V
V_{SDI}, V_{SDO}, V_{NCS}, V_{SCK}, V_{EN}, V_{nFAULT}	Logic input/ouput voltage (EN, SDI, SDO, NCS, SCK, nFAULT)	–0.3	VDD+0.3	V
V_{OUTX}	Output voltage (OUTx) DC condition	–0.3	40	V
	Output voltage (OUTx) AC condition, Iout=1A for t<500ms	-1	40	V

3. ESD Ratings

Symbol	Parameter	Value	Unit
VESD_HBM	Human Body Model (HBM), VMx & VOUTx pins per ANSI/ESDA/JEDEC JS-001	±4000	V
	Human Body Model (HBM), other pins per ANSI/ESDA/JEDEC JS-001	±2000	V
VESD_CDM	Charged device model (CDM), Corner pins, per JEDEC specification JS-002	±750	V
	Charged device model (CDM), other pins, per JEDEC specification JS-002	±500	V

4. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VM	VM supply, normal voltage range	4.5		18	V
	VM supply, extended voltage range (1)	18		Vov	V
	VM supply, over voltage range (2)	Vov		40	V
VDD	VDD supply voltage	3		5.5	V
EN, NCS, SCK, SDO, SDI, nFAULT	Logic input / output voltage	0		5.5	V

(1) Device is capable of full functional operation; however, parameter characteristic is not guarantee, deviation is possible.

(2) No damage to device, and power stage will be disabled during overvoltage range. Full functional operation will resume when battery voltage returns to normal voltage range.

5. Thermal Information

Symbol	Description	Min	Typ	Max	Unit
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature0	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	Thermal resistance, junction to case		2.7		°C/W
Rthja	Thermal resistance, junction to ambient, on 2-layer PCB		62		°C/W
	Thermal resistance, junction to ambient, on 4-layer PCB based on JEDEC standard		30		°C/W

6. Electrical characteristics

T_j = -40°C to 150°C, VM=4.5V to 18V, VDD=3.0 to 5V, unless otherwise specified.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
POWER SUPPLY (VM)						
I_{VM}	VM operating supply current	VM = 13.5V, EN=HIGH, all output off		0.5	2	mA
		VM = 13.5V, EN=HIGH, all high side on			5	mA
I_{VM_SLEEP}	VM sleep current	VM = 13.5V, -40≤Tj≤85°C, EN=LOW, total current of all VM pin			5	μA
V_{UV}	VM undervoltage threshold	VM falls until UVLO triggers	3.6		4.3	V
		VM rises until operation recovers	3.9		4.6	V
V_{UV_HYS}	VM undervoltage hysteresis			400		mV
t_{UV}	VM undervoltage deglitch time	Guaranteed by digital scan		10		us
V_{OV}	VM overvoltage	VM increasing, switch off, OVP_H = 0	22		26	V
		VM decreasing, switch on, OVP_H = 0	20		24	V
		VM increasing, switch off, OVP_H = 1	32		37	V
		VM decreasing, switch on, OVP_H = 1	31		35	V
V_{OV_HYS}	VM overvoltage hysteresis			2		V

t_{OV}	VM overvoltage deglitch time	Guaranteed by digital scan		10		us
VDD SUPPLY INPUT (VDD)						
I_{VDD}	Input current of VDD	EN=High, all outputs off, SPI not active			3	mA
		EN=High, SPI active 5MHz, all high side on			5	mA
I_{VDD_SLEEP}	Input current of VDD in sleep mode	EN=LOW, SPI inactive -40≤Tj≤85°C		1	4	uA
$V_{VDD\_POR\_H}$	POR high threshold	VDD increasing	2.5		3.1	V
$V_{VDD\_POR\_L}$	POR low threshold	VDD decreasing	2.3		2.9	V
LOGIC CONTROL INPUT (EN, NCS, SDI, SCK)						
V_{IL}	Input logic low voltage				0.3*VDD	V
V_{IH}	Input logic high voltage		0.7*VDD			V
V_{HYS}	Input logic hysteresis			0.5		V
R_{PD}	Pulldown resistance	EN, SDI, SCK	50	100	150	kΩ
R_{PU}	Pullup resistance	NCS	50	100	150	kΩ
C_{IN}	Input capacitance	NCS, SDI, SCK pin, Specified by design			15	pF
$T_{Deglitch}$	Deglitch filter on EN falling and rising			10	20	us
T_{WAKE}	Wake-up time	After EN low to high			150	us
NFAULT OUTPUT (OPEN DRAIN)						
V_{OL_nFault}	Output low voltage	I_{OD} = 5mA			0.5	V
I_{LEAK_nFault}	Output high leakage current	V_{OD} = 5V	-1		1	uA
SDO OUTPUT (PUSH PULL)						
V_{OL_SDO}	SDO Output low voltage	Io = 2mA			0.5	V
V_{OH_SDO}	SDO Output high voltage	Io = 2mA	VDD -0.5			V
I_{LEAK_SDO}	SDO tristate leakage	NCS high, 0<V_{SDO}<VDD	-1		1	uA
C_{OUT}	Output capacitance	Specified by design			30	pF
HALF BRIDGE OUTPUS (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6)						

$R_{DS(ON)}$	High-side or Low-side FET on resistance	I = 0.5 A, Tj = 25°C		0.85	1.2	Ω
		I = 0.5 A, Tj = 150°C			1.6	Ω
I_{LEAK_HS}	HS OFF-state leakage	VOUTx = 0V, EN = 1	-2	-1	-	uA
		VOUTx = 0V, EN = 0	-2	-1	-	uA
I_{LEAK_LS}	LS OFF-state leakage	VOUTx = 13.5V, EN = 1, -40≤Tj≤85°C	-	1	5	uA
		VOUTx = 13.5V, EN = 1, -40≤Tj≤150°C	-	1	10	uA
		VOUTx = 13.5V, EN = 0, -40≤Tj≤85°C	-	1	5	uA
		VOUTx = 13.5V, EN = 0, -40≤Tj≤150°C	-	1	10	uA
t_{RISE} t_{FALL}	Output rise time Output fall time High side or low side	VM = 13.5 V, resistive load 100 ohm, HBx_SR = 0		0.6		V/µs
		VM = 13.5 V, resistive load 100 ohm, HBx_SR = 1		2.5		V/µs
t_{PD}	Propagation delay (high side / low side ON/OFF)	HBx_SR = 0		16		µs
		HBx_SR = 1		7		µs
t_{DEAD}	Cross protection time, high to low / low to high	HBx_SR = 0		28		µs
		HBx_SR = 1		7		µs
OVERCURRENT PROTECTION						
I_{OC}	Over current threshold	Half bridge low side	1		1.6	A
		Half bridge high side	-1.6		-1	A
t_{OC}	OC deglitch filter time	OC_Filter bit = 000		10		µs
		OC_Filter bit = 001		5		
		OC_Filter bit = 010		2.5		
		OC_Filter bit = 011		1		
		OC_Filter bit = 100		60		
		OC_Filter bit = 101		40		
		OC_Filter bit = 110		30		
		OC_Filter bit = 111		20		
ON STATE OPEN LOAD DIAGNOSIS						
I_{OL}	Open load threshold	Half bridge low side, HBx_OPL_TH = 0	1.5	10	26	mA
		Half bridge high side, HBx_OPL_TH = 0	-26	-10	-1.5	mA

t_{OL}	Open load filter time	HBx_OPL_TH = 0, guarantee by digital scan	2	3	4	ms
I_{OL_LOW}	Low open load threshold	Half bridge low side, HBx_OPL_TH = 1	0.1	1	2.5	mA
t_{OL_LOW}	Low open load filter time	HBx_OPL_TH = 1, guarantee by digital scan	0.2	0.3	0.4	ms
OFF STATE OPEN LOAD DIAGNOSIS						
I_{PU}	Diag pull up current	HBx_IPUPD_MODE = 0	133	200	320	uA
	Diag pull up current	HBx_IPUPD_MODE = 1	0.66	1	1.5	mA
I_{PD}	Diag pull down current	HBx_IPUPD_MODE = 0	400	600	900	uA
	Diag pull down current	HBx_IPUPD_MODE = 1	2	3	4.5	mA
V_{STA_HB}	Off state status threshold	OUTx pin	0.54 *VDD	0.6* VDD	0.66*VDD	V
THERMAL PROTECTION						
OT_{WARN}	Thermal warning temperature		120	140	160	°C
T_{HYS_OTW}	Thermal warning hysteresis			20		°C
OT_{SD}	Thermal shutdown temperature		150	170	190	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis			20		°C
SPI AC TIMINGS						
T_{cll}	Minimum time CLK = LOW (5)	Application info	85			ns
T_{clh}	Minimum time CLK = HIGH (4)	Application info	85			ns
T_{pcld}	Propagation delay (SCLK to data at SDO active) (B)	Cload=30pF			30	ns
T_{lead}	CLK change L/H after NCS = LOW (2)	Application info	100			ns
T_{scld}	SDI input setup time (CLK change H/L after SDI data valid) (F)	Application info	30			ns

T_{hcld}	SDI input hold time (SDI data hold after CLK change H/L) (C)	Application info	30			ns
T_{sclch}	CLK low before NCS low (1)	Application info	125			ns
T_{lag}	CLK low before NCS high (6)	Application info	100			ns
T_{hclch}	CLK high after NCS high	Application info	100			ns
T_{onncs}	NCS min high time (9)	Application info	1			us
T_{pchdz}	NCS L/H to SDO @ high impedance (E)	Cload=30pF			75	ns
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info			5	MHz

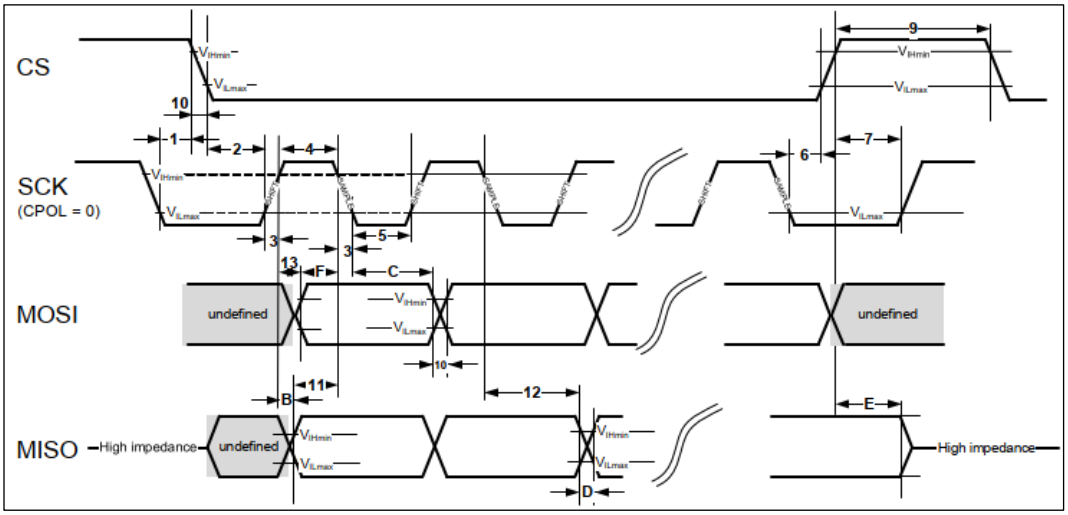

Figure 3. SPI timing diagram

7. Functional description

7.1. VM & VM UV / OV protection

VM is the supply voltage, range from 4.5v to 36v with typical case 13.5v power supply. It is recommended to put at both 100nF ceramic and >10uF bulk electrolytic capacitor closed to each VM pin.

When VM power supply pin voltage falls below the undervoltage threshold (V_{UV}) over 10us typ. undervoltage deglitch time, half bridge outputs OUTx becomes OFF. When VM rise above the $V_{UV,}$ the device automatically resumes operation.

When VM power supply pin voltage rises above the overvoltage threshold (V_{OV}) over 10us typ. overvoltage deglitch time, half bridge outputs OUTx becomes OFF. When VM decrease under the $V_{OV,}$ the device automatically resumes operation. OVP_H register bit set the two different VM input overvoltage threshold.

7.2. VDD

VDD pin accepts wide supply range from 3v to max 5.5v which intends for the compatibility with both 3.3v and 5v system supply. 100nF X7R ceramic capacitor is suggested to put closed to VDD pin.

Internal block, SPI interface, digital block will be inactive when VDD drops below $V_{VDD\_POR\_L}$, so including charge pump and all half bridge drivers are switched off. Once VDD > $V_{VDD\_POR\_H}$, internal digital is reset, and status register NPOR bit is set to 0 and can be cleared to 1 by SPI readout (if RD_CLR_EN=1) or CLR_FLT = 1 command.

7.3. EN input

The EN pin signal is common for all output channels. When it is driven low, internal logic / register is reset, charge pump / all outputs are disabled, and device enter sleep mode.

After EN transition from low to high at VDD > $V_{VDD\_POR\_H}$, device come out sleep mode at finishing internal POR and NPOR=0.

A T_{WAKE} time shall be wait for charge pump reach regulated voltage once device move from sleep to normal operation.

7.4. Half bridge output stage, OUT1 ~ OUT6

The half bridge drivers are designed to drive DC motor or general used inductive/resistive load like LED.

The power stage outputs (out1~out6) can be in parallel to support higher load current.

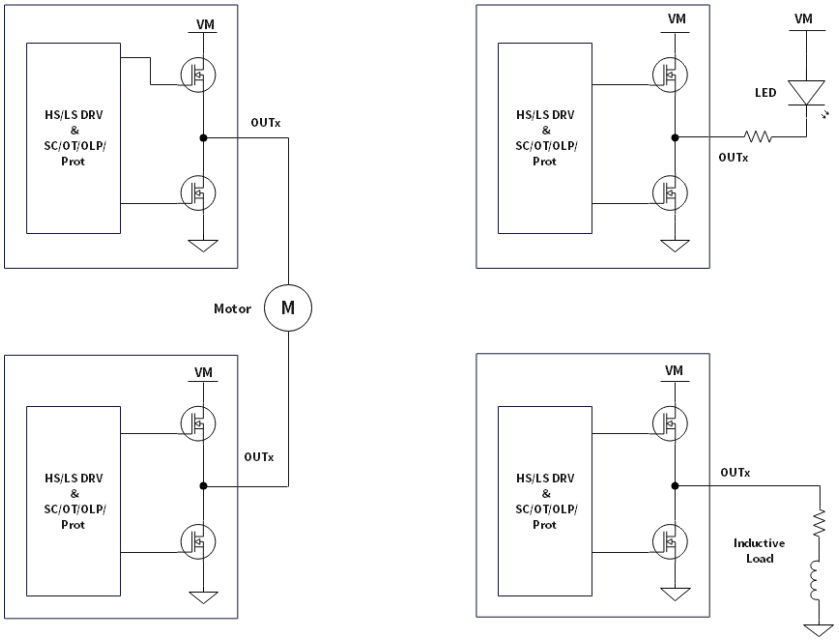

Figure 4. Power stage output block diagram

7.4.1. SPI Control ON/OFF operation

To directly operate half bridge output by only SPI ON/OFF control, the two group register as below shall be controlled in following steps.

1. HBx_PWM_EN bit configuration in register HB_PWM_CTRL1 and FW_PWM_CTRL_2
2. HBx_HS_EN or HBx_LS_EN bit configuration in register HB_CTRL1 / HB_CTRL2 / CTRL3

Note:

- HBx_PWM_EN bit shall be configured or keep default value '0' for SPI control ON/OFF operation

- One specific half bridge, HBx_HS_EN and HBx_LS_EN shall not be '1' at the same time, otherwise, the specific half bridge will be HIZ until this same bridge HS and LS control bit both high condition is removed

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An example of activation of HB1_HS / HB1_LS and HB2_HS / HB2_LS to drive motor by SPI control as table 7.4.1 shown

Table 7.4.1. Half bridge SPI control register setting example

EN	HB1 register setting	HB2 register setting	OUT1	OUT2
LOW	x	x	HIZ	HIZ
High	HB1_PWM_EN=0 HB1_HS_EN=0 HB1_LS_EN=0	HB2_PWM_EN=0 HB2_HS_EN=0 HB2_LS_EN=0	HIZ	HIZ

High	HB1_PWM_EN=0 HB1_HS_EN=1 HB1_LS_EN=0	HB2_PWM_EN=0 HB2_HS_EN=0 HB2_LS_EN=1	High	Low
High	HB1_PWM_EN=0 HB1_HS_EN=0 HB1_LS_EN=1	HB2_PWM_EN=0 HB2_HS_EN=0 HB2_LS_EN=1	Low	Low
High	HB1_PWM_EN=0 HB1_HS_EN=0 HB1_LS_EN=1	HB2_PWM_EN=0 HB2_HS_EN=1 HB2_LS_EN=0	Low	High
High	HB1_PWM_EN=0 HB1_HS_EN=1 HB1_LS_EN=0	HB2_PWM_EN=0 HB2_HS_EN=1 HB2_LS_EN=0	High	High

7.4.2. PWM control operation

PWM control is based on internal digital PWM generator and map control block. It is suggested to set following registers

- PWM frequency / duty cycle / map control

  (1) PWMx_FREQ bit in PWM_FREQ_CTRL1 / PWM_FREQ_CTRL2 registers
  Total 8 PWM generator, 2bit configuration for each PWM freq as (80Hz / 100Hz / 200Hz / 2000Hz) in +/-30% variation for full operating and temperature range.

  (2) PWMx_DUTY_CYCLE bit in PWM_DC_CTRL1~PWM_DC_CTRL8 registers
  8bit configuration of PWMx_DUTY_CYCLE define the duty cycle of generated PWMx as 100%*BIT value /255

  (3) HBx_PWM_MAP bit in PWM_MAP_CTRL1~PWM_MAP_CTRL6 registers
  3bit for each Half bridge, which allows independent and flexible selection from PWM1~PWM8

- Half bridge driver setting for PWM

  (1) HBx_PWM_EN bit in HB_PWM_CTRL1, FW_PWM_CTRL2
  HBx_PWM_EN bit changed to '1' will enable the selected half bridge operation control by mapped PWM

  (2) HBx_HS_EN / HBx_LS_EN in HB_CTRL1~HB_CTRL3
  Set HBx_HS_EN or HBx_LS_EN bit at '1' to enable the PWM activated Power FET stage.

- Active / passive freewheeling setting in PWM

  (1) HBx_FW bit in FW_CTRL_1, FW_PWM_CTRL_2 registers

  When the particular half bridge channel is chosen to use PWM, it is also possible to select the active or passive freewheeling option for the half bridge channel, by HBx_FW control bit.

An example of active HB1 SPI ON and HB2 LS in PWM mode / HB2 HS in passive or active freewheeling to drive motor / inductive load is shown in figure 5.

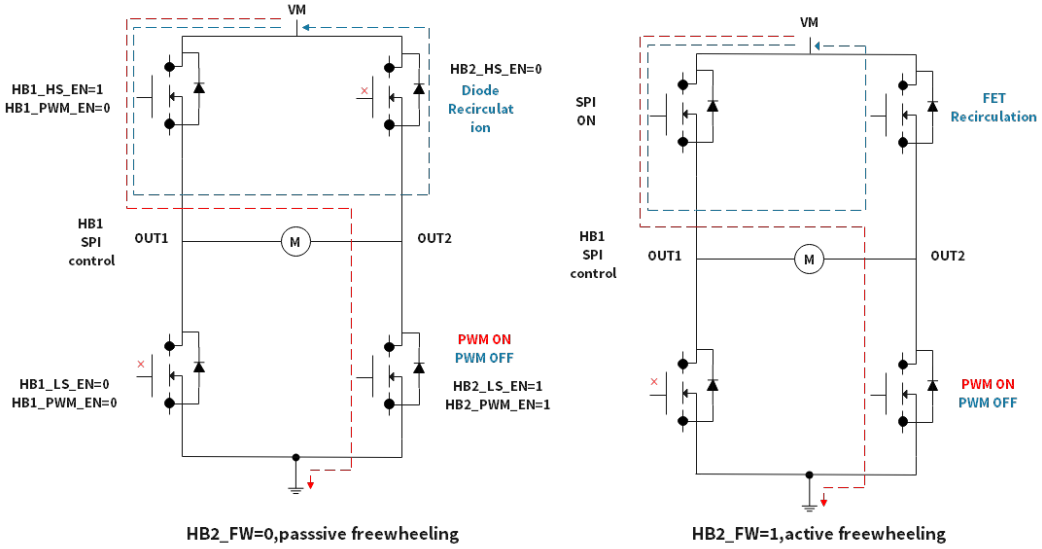


Figure 5. Passive freewheeling vs. active freewheeling

Note:

- Active freewheeling function automatically turns on the freewheeling FET, after the driving FET turns off at PWM ON->OFF and cross protection time t_{DEAD} elapsed

- HBx_FW bit value is not effective when HBx_PWM_EN bit is configured as SPI control ON/OFF

- PWM enable / disable

  (1) PWMx_DIS bit in HB_PWM_CTRL2

  PWM channel independent enable / disable bit

Example of PWM mode control register setting and steps

1. Configure PWMx_DIS bit into '1' (PWM stopped and off) for selected PWM channel
2. Configure active or passive free-wheeling in FW_CTRL register
3. Assign the PWM channel for selected half-bridge output in PWM_MAP_CTRL register
4. Configure the PWM frequency in PWM_FREQ_CTRL register
5. Configure the PWM duty cycle in PWM_DC_CTRL register
6. Assign the channel driven mode SPI on/off or PWM operation by HBx_PWM_EN in HB_PWM_CTRL register
7. Select the channel HS or LS to be driven by HBx_HS_EN or HBx_LS_EN in HB_CTRL register
8. Active and begin the PWM by PWMx_DIS bit to '0

7.4.3. Output in parallel

For SPI ON/OFF control in parallel, it is recommended to select half bridge channel in same register, ie HB1, HB2, HB3, HB4 HS / LS control bit are all in HB_CTRL_1 register, while HB5, HB6 are in HB_CTRL_2.

For PWM control in parallel, to ensure the HS or LS activated simultaneously, it is mandatory to put the PWM activation in the last step for PWM mode control register setting.

7.5. Half bridge protection and diagnosis

7.5.1. Overcurrent protection

The integrated overcurrent protection function provides the half bridge high side against short to ground or half bridge low side against short to battery.

When the current pass the half bridge high side (VM->highside->OUTx) or flow into the half bridge low side (OUTx->low side->GND), once I_{OC} overcurrent threshold is exceeded, an overcurrent deglitch filter t_{OC} starts and internal circuit limits current at I_{LIM}.

Upon the overcurrent condition last until t_{OC} expiration, the particular half bridge (including high side and low side) is disabled. The OC status bit shall report the corresponding HS or LS which trigger OC. nFAULT pin also asserts low if OC_MASK_FLT is set '0'.

For example, if only HB1 LS is short to battery and detected, OC_STA_1 register HB1_LS_OC bit is asserted while HB1_HS_OC bit not affected, for output stage, both HB1 HS and LS are disabled.

To resume normal driving, besides the overcurrent condition disappear, it is also required to clear the OC status bit by SPI reading (RD_CLR_EN=1) or writing DIAG_CLR bit '1' to trigger clear fault command.

Note:

1. Even the half bridge output is disabled due to overcurrent protection mechanism, the HBx_HS_EN or HBx_LS_EN bit remains previous state, unless user change the value through SPI.

2. During overcurrent fault handling process, it is suggested to first reset the HBx_HS_EN or HBx_LS_EN bit to 0, then clear the OC status bit by SPI command, the last is to re-enable HBx_HS_EN or HBx_LS_EN bit. For example, HB1 previous state is HS ON and HS OC, so the procedure of HB1 OC fault handling is first writing HB1_HS_EN bit =0, then sending DIAG_CLR '1' to clear HB1 OC fault, the last is to set HB1_HS_EN=1 to enable HB1 HS again.

3. When device operate in high voltage (e.g. > 28v), short t_{OC} (OC_Filter bit in OPL_OC_CTRL3 register) is suggested.

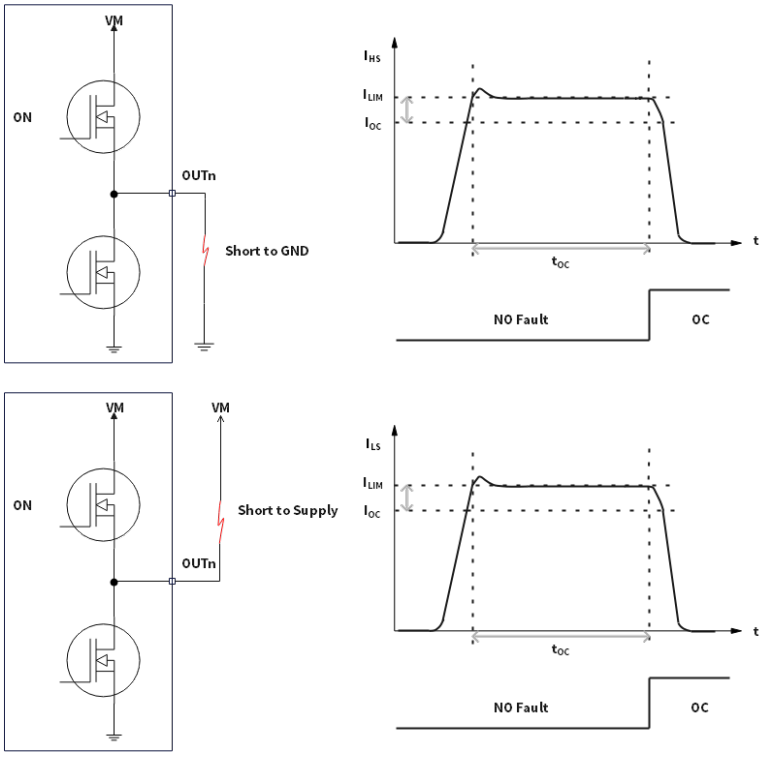


Figure 6. High-Side Switch and Low-Side Switch - Short Circuit and Overcurrent Protection

Anyhow if overcurrent condition short than t_{OC} deglitch filter, the OC event is not confirmed, and HB driver keeps normal status.

The device also provides two slew rate options in case half bridge output stage turn off caused by OC protection. High slew rate turns off (typ 2.5v/us) used in default for OC as OC_OFF_SR bit in OPL_OC_CTRL_3 is set to '0', while slow slew rate turns off in OC condition (OC_OFF_SR=1) shall be carefully evaluated for device operating ambient condition and power dissipation.

7.5.2. Open load in ON state

The load current is monitored in each activated output stage for open load detection in ON state.

If the load current is below open load detection threshold IOL for at least typ.3ms (t_{OL}), the corresponding open load bit is set in status register.

The device also provide HBx_OPL_TH selection bit for lower open load threshold IOL_LOW and the corresponding filter time t_{OL_LOW} , which targets for low current loads ie. LED.

Furthermore, two bits, OPL_HB_ACT bit and OPL_mask_FLT bit in OPL_OC_CTRL_2 register, can be configured for open load fault reaction.

- OPL_HB_ACT bit determines whether half bridge output status is impacted by ON state open load fault. Default value '0' will disable faulty half bridge HS and LS, while setting the bit value to '1' can choose open load only as information flag and half bridge control / operation not impacted.

- OPL_mask_FLT bit determines whether nFault output pin status is impacted by ON state open load fault. Default value '0' unmasks and generates nFault low at open load detected, while changing to '1' will mask open load fault and doesn't report on nFault output.

User can clear the OL status bit by SPI reading (RD_CLR_EN=1) or writing DIAG_CLR bit '1' to trigger clear fault command to determine whether open load is still present or disappeared.

Note:

1. For DC motor application, it is recommended to use SPI ON/OFF short activation of outputs (e.g. 4ms) to test DC motor open load status without changing the mechanical state of motor.

2. For LED load application, PWM control might be used, the lower open load threshold and shorter filter shall be chosen. During PWM OFF/freewheeling state, open load detection is blanked.

3. Additionally, the low open load threshold function for LED application is implemented only on low-side. The user has to enable the low current open load mode for the corresponding low-side and connect the LED load in low side proper operation way.

4. Each half bridge ON state open load detection can be disabled by HBx_OPL_DIS bit in OPL_CTRL_1/2 register, in case ON state open load diagnosis is not required.

7.5.3. OFF-state diagnosis

Each half bridge OUTx integrates internal pull-up current / pull-down current and comparator for off-state diagnosis as figure 7 shown.

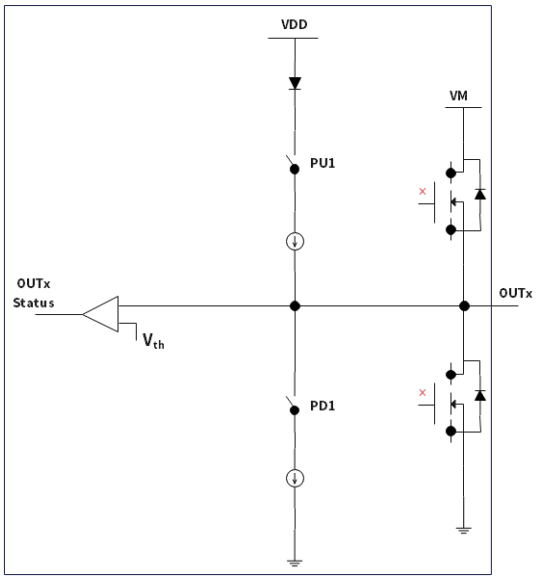


Figure 7. Half – Bridge diagnosis OFF-STATE

Pull up current or pull down current are individually controlled as enable / disable by register OPL_CTRL_5 and OPL_CTRL_6 bit setting values.

The OUTx pin voltage is compared with VSTA_HB to determine its off-state logic status (HIGH or LOW) in real time and reported in HB_STA1 register.

Note:

- NSD8306/NSD8306A can be used in various load connection topologies, Half bridge/H-bridge/LS/HS connection. To diagnosis the OUTx external connection status (normal, short to battery, short to ground, open load), it is suggested to follow the off-state diagnosis step of NSD8306/NSD8306A application note / FAQ document and run the recommended the pull-up / down current enable/disable sequence to read back the OUTx pin voltage status combination using microcontroller.

7.5.4. Overtemperature

To protect power stage from overheat, dedicated thermal sensor is placed close to each half bridge power stage, if the temperature increases above the OTwarn, a temperature warning flag is set in SPI STA_0 register, half bridge output operation is not impacted. Once the sensed temperature over the second OT_{SD} threshold, the corresponding OTSD flag is set and power MOSFET channel is automatically disabled.

nFAULT pin can be configured for OTwarn event report upon OTW_MASK_FLT bit setting. Anyhow OTSD will always asserted nFAULT to low.

OTwarn and OTSD flag bit are latched. In order to reactive the output stage after OTSD and release nFAULT pin, the temperature drops below T_{SD}-$T_{HYS,}$ and the thermal shutdown OTSD bit shall be clear by SPI command.

7.5.5. Fault Protection Summary

EVENT	VM			VDD	EN	Thermal		Load current		
	OV1 t>tov	OV2 t>tov	UV	UV	H->L	OVER TEMPERATURE Warning	OVER TEMPERATURE shutdon	OC	OL in ON	
	SPI CTRL_0 register OVP_H bit					OTW_MASK_FLT		OC_MASK_FLT	OPL_HB_ACT OPL_mask_FLT	
FLAG READ BY SPI	VM_OV	VM_OV	VM_UV	NPOR		OTWARN	OTSD	HBx_HS_OC HBx_LS_OC	HBx_HS_OPL HBx_LS_OPL	
Internal supply	○	○	○	▲	▲	○	○	○	○	
Internal OSC	○	○	○	▲	▲	○	○	○	○	
Charge pump	○	○	▲	▲	▲	○	○	○	○	
OUT1~OUT12	▲	▲	▲	▲	▲	○	▲	▲*1	▲*2 *1	
nFault	△	△	△	-	-	△*3	△	△*4	△*5	
SPI communication	○	○	○	▲	▲	○	○	○	○	
SPI REGISTERS	○	○	○	▲	▲	○	○	○	○	

x	detection	*1	The fault output off state, caused by OC or OL in ON, is latched until the corresponding retart condition is met.
○	normal operation	*2	On state open load switch off the corresponding HB channel both HS and LS output, if OPL_HB_ACT bit =0.
-	not active	*3	OTW_MASK_FLT =1 means that overtemperature warning triggers nFAULT low
●	partial functionality	*4	OC_MASK_FLT =0 unmasks and report on nFAULT if OC happens
▲	stop/reset	*5	OPL_mask_FLT=0 unmasks and report on nFAULT if Open load on state detected
△	active LOW		

7.6. SPI interface

The following table summarizes the SPI interface designed.

Table 7.6.1 – SPI Interface quick look

Parameter	Description
Protocol	in frame
Single Frame Length	16 bit, MSB first
Frame protection	frame length check
Max. Frequency	5 MHz
CPOL	0
CPHA	1
Master/Slave configuration	Slave

The falling edge of NCS defines the start of the SPI frames. It samples the SDI line at the falling edge of SCK, while the output data is shifted out on SDO line at the rising edge of SCK (CPOL='0' CPHA = '1'). The end of SPI frame is defined by a rising edge of NCS.

7.6.1. Frame Length Check

For each command received, the SPI peripheral checks the number of clock edges at SCK pin. If the total number of edges is not a multiple of 16, the frame content is discarded and an SPI_ERR bit will be returned upon next iteration.

7.6.2. Error Frame

In case one of the following error occurs, the SPI_ERR diagnosis bit will be returned upon next communication iteration:

- Frame Length error
- Invalid address

7.6.3. SPI Frame structure

Each SDI input frame has 16 bits with the following structure:

- 2 operation command bit C1 / C0 ‘00’ for write operation, ‘01’ for read operation
- 6 ADDRESS bits
- 8 DATA bits

	MSB LSB								
BIT	15	14	13	12	11	10	9	8	[7:0]
SDI	C1	C0	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	DATA

Register frame SDO responses the selected address and register content bit values. It has with the following structure:

- 2bit ‘1’ , reserved
- 6bits, UV event / OV event , Overtemperature, NPOR and power stage status OC, OL
- 8 DATA bits

	MSB LSB								
BIT	15	14	13	12	11	10	9	8	[7:0]
SDO	1	1	OT	OL	OC	UV	OV	NPOR	DATA

Note:

For SPI write operation, the SDO response data is the value which is currently written to.

For SPI read operation, the SDO response data is the value which register address has been read.

7.6.4. Parallel and daisy chain capability

SPI communication between microcontroller (SPI master) and multiple these devices (slave) can be operated in parallel or in daisy chain.

Parallel operation: several slave devices are connected to one SPI channel, which share communication lines SDI, SDO and SCK, but every slave connects dedicated own NCS.

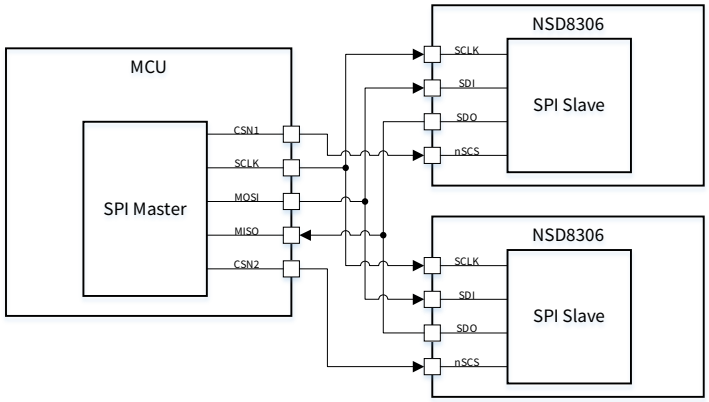


Figure 8 Without daisy chain, in parallel operation diagram

Daisy chain operation: multi devices are connected with shared one NCS and SCK, while each device SDI and SDO are daisy-chain connected.

Daisy chain operation: multi devices are connected with shared one NCS and SCK, while each device SDI and SDO are daisy-chain connected. An example of 3 devices in daisy chain as below figure 9:

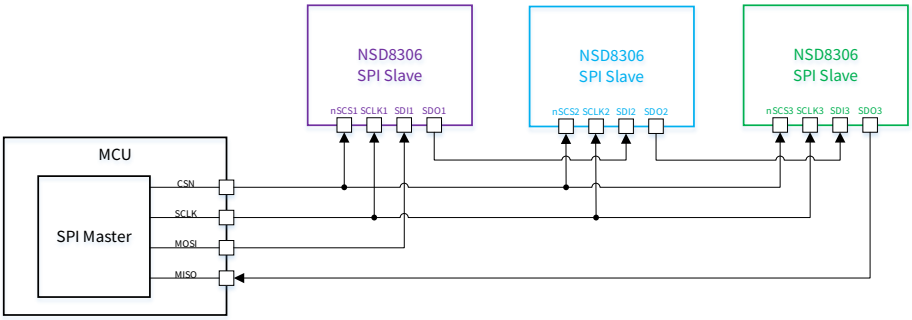


Figure 9 Daisy Chain Operation for 3 Devices

The SPI format for daisy chain SPI operation as below, A1~A3, D1~D3, S1~S3, R1~R3 have same meaning/definition with single device operation described

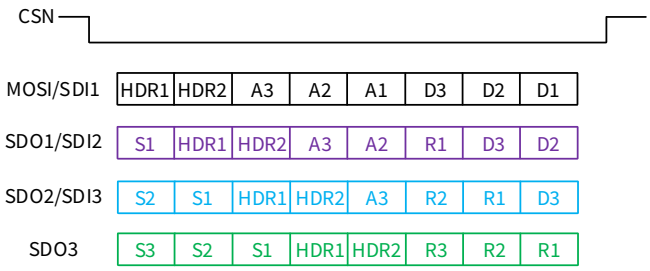


Figure 10 SPI Format for 3 Devices Daisy Chain

There are two header bytes dedicated for daisy chain operation

- HDR1 byte contain information of the number of devices connected in the chain by N0~N5 bits, so device support up to 63 devices, other bits are fixed
- HDR2 byte contain CLR bit which can trigger SPI clear command for all device in daisy chain, other bits are fixed (bit7 and bit6) or not care(bit0~bit4)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HDR1	1	0	N5	N4	N3	N2	N1	N0

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HDR2	1	0	CLR	X	X	X	X	X

Figure 11 Daisy Chain Header Bytes Format

Note: Internal logic will count number of status bytes it receives before HDR1 and HDR2 to know the position of itself in the chain, also by HDR1 it knows how many devices in the chain, so it only loads the relevant address and data byte in its buffer and bypass the other bytes.

7.6.5. Registers map

SECT	REG_NAME	REG_ADDR	bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Status registers	STA_0	0x00	Reserved	OTSD	OTWARN	OPL	OC	VM_UV	VM_OV	NPOR
	OC_STA_1	0x01	HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
	OC_STA_2	0x02	Reversed				HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
	OPL_STA_1	0x04	HB4_HS_OPL	HB4_LS_OPL	HB3_HS_OPL	HB3_LS_OPL	HB2_HS_OPL	HB2_LS_OPL	HB1_HS_OPL	HB1_LS_OPL
	OPL_STA_2	0x05	Reversed				HB6_HS_OPL	HB6_LS_OPL	HB5_HS_OPL	HB5_LS_OPL
	HB_STA_1	0x2B	Reversed		HB6_STA	HB5_STA	HB4_STA	HB3_STA	HB2_STA	HB1_STA
Control registers	GEN_CTRL_0	0x07	OFF_DIAG_COMP_EN	DEVICE_ID			OC_MASK_FLT	OTW_NMASK_FLT	OVP_H	DIAG_CLR
	HB_CTRL_1	0x08	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
	HB_CTRL_2	0x09	Reversed				HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
	HB_PWM_CTRL1	0x0B	Reversed		HB6_PWM_EN	HB5_PWM_EN	HB4_PWM_EN	HB3_PWM_EN	HB2_PWM_EN	HB1_PWM_EN
	HB_PWM_CTRL2	0x0C	PWM8_DIS	PWM7_DIS	PWM6_DIS	PWM5_DIS	PWM4_DIS	PWM3_DIS	PWM2_DIS	PWM1_DIS
	FW_CTRL_1	0x0D	Reversed		HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW
	PWM_MAP_CTRL_1	0x0F	Reserved	Reserved	HB2_PWM_MAP			HB1_PWM_MAP		
	PWM_MAP_CTRL_2	0x10	Reserved	Reserved	HB4_PWM_MAP			HB3_PWM_MAP		
	PWM_MAP_CTRL_3	0x11	Reserved	Reserved	HB6_PWM_MAP			HB5_PWM_MAP		
	PWM_FREQ_CTRL1	0x13	PWM4_FREQ		PWM3_FREQ		PWM2_FREQ		PWM1_FREQ	
	PWM_FREQ_CTRL2	0x14	PWM8_FREQ		PWM7_FREQ		PWM6_FREQ		PWM5_FREQ	
	PWM_DC_CTRL1	0x15	PWM1_DUTY_CYCLE							
	PWM_DC_CTRL2	0x16	PWM2_DUTY_CYCLE							
	PWM_DC_CTRL3	0x17	PWM3_DUTY_CYCLE							
	PWM_DC_CTRL4	0x18	PWM4_DUTY_CYCLE							

	PWM_DC_CTRL5	0x19	PWM5_DUTY_CYCLE						
	PWM_DC_CTRL6	0x1A	PWM6_DUTY_CYCLE						
	PWM_DC_CTRL7	0x1B	PWM7_DUTY_CYCLE						
	PWM_DC_CTRL8	0x1C	PWM8_DUTY_CYCLE						
	HB_SR_CTRL_1	0x1D	Reversed		HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
	HB_SR_CTRL_2	0x1E	Reversed							
	OPL_CTRL_1	0x1F	Reversed		HB6_OPL_DIS	HB5_OPL_DIS	HB4_OPL_DIS	HB3_OPL_DIS	HB2_OPL_DIS	HB1_OPL_DIS
	OPL_OC_CTRL_2	0x20	OPL_mask_FLT	OPL_HB_ACT	Reserved	OC_OFF_SR	reversed			
	OPL_OC_CTRL_3	0x21	OC_FILTER			Reserved	reversed			
	OPL_CTRL_4	0x22	Reversed		HB6_OPL_TH	HB5_OPL_TH	HB4_OPL_TH	HB3_OPL_TH	HB2_OPL_TH	HB1_OPL_TH
	OPL_CTRL_5	0x23	Reversed							
	OPL_CTRL_6	0x24	Reversed							
	GEN_CTRL_1	0x25	SS_MOD		SS_DEV	RD_CLR_EN	unlock	SPI_ERR	Reversed	
	OPL_CTRL_5	0x28	HB4_OFF_PU_EN	HB4_OFF_PD_EN	HB3_OFF_PU_EN	HB3_OFF_PD_EN	HB2_OFF_PU_EN	HB2_OFF_PD_EN	HB1_OFF_PU_EN	HB1_OFF_PD_EN
	OPL_CTRL_6	0x29	Reversed				HB6_OFF_PU_EN	HB6_OFF_PD_EN	HB5_OFF_PU_EN	HB5_OFF_PD_EN
	OPL_CTRL_8	0x2D	Reversed		HB6_IPUPD_MODE	HB5_IPUPD_MODE	HB4_IPUPD_MODE	HB3_IPUPD_MODE	HB2_IPUPD_MODE	HB1_IPUPD_MODE
	OPL_CTRL_9	0x2E	OCPH_CONF	VM_OVPH_CONF	IDCH_CONF	TDEAD_MON_EN	Reversed			

7.6.6. SPI – control and status registers

Table 7.6.1 STA_0 status register (REG_ADDR = 0x00)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	OTSD	OTWARN	OPL	OC	VM_UV	VM_OV	NPOR
Operation Type	RO	RLR	RLR	RO	RO	RLR	RLR	RLR
Default	0	0	0	0	0	0	0	1

Table 7.6.2 STA_0 status register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6	OTSD	0: No over temperature shutdown happen (default value) 1: over temperature shutdown detected. Error latched and all outputs disabled
5	OTWARN	0: No over temperature warning happen (default value) 1: over temperature warning detected
4	OPL	0: No open load detected (default value) 1: open load detected in at least one of power stages.
3	OC	0: No overcurrent detected (default value) 1: overcurrent detected in at least one of power stages. Error latched and corresponding outputs disabled
2	VM_UV	0: No VM undervoltage detected (default value) 1: VM undervoltage detected. Error latched and all outputs disabled
1	VM_OV	0: No VM overvoltage detected (default value) 1: VM overvoltage detected. Error latched and all outputs disabled
0	NPOR	0: POR due to VDD supply or EN (default value) 1: No POR. Note: NPOR bit remains '0' until cleared through the DIAG_CLEAR bit or SPI readout (if RD_CLR_EN=1)

Table 7.6.3 OC_STA_1 status register (REG_ADDR = 0x01)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
Operation Type	RLR	RLR	RLR	RLR	RLR	RLR	RLR	RLR
Default	0	0	0	0	0	0	0	0

Table 7.6.4 OC_STA_1 status register description

Bit	Field Name	Description
7	HB4_HS_OC	0: No overcurrent in HB4 high side detected (default value) 1: overcurrent detected in HB4 high side. Error latched, HB4 HS is disabled.
6	HB4_LS_OC	0: No overcurrent in HB4 low side detected (default value) 1: overcurrent detected in HB4 low side. Error latched, HB4 LS is disabled.
5	HB3_HS_OC	0: No overcurrent in HB3 high side detected (default value) 1: overcurrent detected in HB3 high side. Error latched, HB3 HS is disabled.
4	HB3_LS_OC	0: No overcurrent in HB3 low side detected (default value) 1: overcurrent detected in HB3 low side. Error latched, HB3 LS is disabled.
3	HB2_HS_OC	0: No overcurrent in HB2 high side detected (default value) 1: overcurrent detected in HB2 high side. Error latched, HB2 HS is disabled.

2	HB2_LS_OC	0: No overcurrent in HB2 low side detected (default value) 1: overcurrent detected in HB2 low side. Error latched, HB2 LS is disabled.
1	HB1_HS_OC	0: No overcurrent in HB1 high side detected (default value) 1: overcurrent detected in HB1 high side. Error latched, HB1 HS is disabled.
0	HB1_LS_OC	0: No overcurrent in HB1 low side detected (default value) 1: overcurrent detected in HB1 low side. Error latched, HB1 LS is disabled.

Table 7.6.5 OC_STA_2 status register (REG_ADDR = 0x02)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved				HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
Operation Type	RO				RLR	RLR	RLR	RLR
Default	0				0	0	0	0

Table 7.6.6 OC_STA_2 status register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5		
4		
3	HB6_HS_OC	0: No overcurrent in HB6 high side detected (default value) 1: overcurrent detected in HB6 high side . Error latched, HB6 HS is disabled.
2	HB6_LS_OC	0: No overcurrent in HB6 low side detected (default value) 1: overcurrent detected in HB6 low side . Error latched, HB6 LS is disabled.
1	HB5_HS_OC	0: No overcurrent in HB5 high side detected (default value) 1: overcurrent detected in HB5 high side . Error latched, HB5 HS is disabled.
0	HB5_LS_OC	0: No overcurrent in HB5 low side detected (default value) 1: overcurrent detected in HB5 low side . Error latched, HB5 LS is disabled.

Table 7.6.7 OPL_STA_1 status register (REG_ADDR = 0x04)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	HB4_HS_OPL	HB4_LS_OPL	HB3_HS_OPL	HB3_LS_OPL	HB2_HS_OPL	HB2_LS_OPL	HB1_HS_OPL	HB1_LS_OPL
Operation Type	RLR	RLR	RLR	RLR	RLR	RLR	RLR	RLR
Default	0	0	0	0	0	0	0	0

Table 7.6.8 OPL_STA_1 status register description

Bit	Field Name	Description
7	HB4_HS_OPL	0: No ON state open load in HB4 high side detected (default value) 1: ON state open load detected in HB4 high side . Error latched
6	HB4_LS_OPL	0: No ON state open load in HB4 low side detected (default value) 1: ON state open load detected in HB4 low side . Error latched
5	HB3_HS_OPL	0: No ON state open load in HB3 high side detected (default value) 1: ON state open load detected in HB3 high side . Error latched
4	HB3_LS_OPL	0: No ON state open load in HB3 low side detected (default value) 1: ON state open load detected in HB3 low side . Error latched
3	HB2_HS_OPL	0: No ON state open load in HB2 high side detected (default value) 1: ON state open load detected in HB2 high side . Error latched

2	HB2_LS_OPL	0: No ON state open load in HB2 low side detected (default value) 1: ON state open load detected in HB2 low side . Error latched
1	HB1_HS_OPL	0: No ON state open load in HB1 high side detected (default value) 1: ON state open load detected in HB1 high side . Error latched
0	HB1_LS_OPL	0: No ON state open load in HB1 low side detected (default value) 1: ON state open load detected in HB1 low side . Error latched

Table 7.6.9 OPL_STA_2 status register (REG_ADDR = 0x05)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved				HB6_HS_OPL	HB6_LS_OPL	HB5_HS_OPL	HB5_LS_OPL
Operation Type	RO				RLR	RLR	RLR	RLR
Default	0				0	0	0	0

Table 7.6.10 OPL_STA_2 status register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5		
4		
3	HB6_HS_OPL	0: No open load in HB6 high side detected (default value) 1: open load detected in HB6 high side . Error latched
2	HB6_LS_OPL	0: No open load in HB6 low side detected (default value) 1: open load detected in HB6 low side . Error latched
1	HB5_HS_OPL	0: No open load in HB5 high side detected (default value) 1: open load detected in HB5 high side . Error latched
0	HB5_LS_OPL	0: No open load in HB5 low side detected (default value) 1: open load detected in HB5 low side . Error latched

Table 7.6.11 HB_STA_1 status register (REG_ADDR = 0x2B)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB6_STA	HB5_STA	HB4_STA	HB3_STA	HB2_STA	HB1_STA
Operation Type	RO		RO	RO	RO	RO	RO	RO
Default	0		0	0	0	0	0	0

Table 7.6.12 HB_STA_1 status register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5	HB6_STA	0: HB6 output voltage status low (<Vth) 1: HB6 output voltage status high(>Vth)
4	HB5_STA	0: HB5 output voltage status low (<Vth) 1: HB5 output voltage status high(>Vth)
3	HB4_STA	0: HB4 output voltage status low (<Vth) 1: HB4 output voltage status high(>Vth)
2	HB3_STA	0: HB3 output voltage status low (<Vth) 1: HB3 output voltage status high(>Vth)

1	HB2_STA	0: HB2 output voltage status low (<Vth) 1: HB2 output voltage status high(>Vth)
0	HB1_STA	0: HB1 output voltage status low (<Vth) 1: HB1 output voltage status high(>Vth)

Table 7.6.13 GEN_CTRL_0 control register (REG_ADDR = 0x07)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	OFF_DIAG_COMP_EN	DEVICE_ID			OC_MASK_FLT	OTW_NMASK_FLT	OVP_H	DIAG_CLR
Operation Type	RW	RO			RW	RW	RW	WO
Default	0	Device related			0	0	0	0

Table 7.6.14 GEN_CTRL_0 control register description

Bit	Field Name	Description
7	OFF_DIAG_COMP_EN	0: all half bridge OFF state diagnosis comparators are disabled; and comparator output keeps default value 0 (default value) 1: all half bridge OFF state diagnosis comparators are enabled
6	DEVICE_ID	100 = NSD8306 101 = NSD8308 110 = NSD8310 111 = NSD8312 others reversed
5		
4		
3	OC_MASK_FLT	0: overcurrent unmasked, reported on nfault (default value) 1: overcurrent event is masked, not reported on nfault
2	OTW_NMASK_FLT	0: overtemperature warning masked, not reported on nfault (default value) 1: overtemperature warning unmasked, reported on nfault
1	OVP_H	0: VM overvoltage voltage threshold at >21v (default value) 1: Higher overvoltage protection threshold, VM up to >32v
0	DIAG_CLR	0: no action - clear all fault (default value) 1: Trigger action - clear all fault Note: DIAG_CLR bit is auto clear bit and always read as '0'. Every time writing '1' triggers single pulse to clear diagnosis result.

Table 7.6.15 HB_CTRL_1 control register (REG_ADDR = 0x08)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Table 7.6.16 HB_CTRL_1 control register description

Bit	Field Name	Description
7	HB4_HS_EN	0: HB4 high side disabled (default value) 1: HB4 high side enabled
6	HB4_LS_EN	0: HB4 low side disabled (default value) 1: HB4 low side enabled
5	HB3_HS_EN	0: HB3 high side disabled (default value) 1: HB3 high side enabled
4	HB3_LS_EN	0: HB3 low side disabled (default value) 1: HB3 low side enabled

3	HB2_HS_EN	0: HB2 high side disabled (default value) 1: HB2 high side enabled
2	HB2_LS_EN	0: HB2 low side disabled (default value) 1: HB2 low side enabled
1	HB1_HS_EN	0: HB1 high side disabled (default value) 1: HB1 high side enabled
0	HB1_LS_EN	0: HB1 low side disabled (default value) 1: HB1 low side enabled

Table 7.6.17 HB_CTRL_2 control register (REG_ADDR=0x09)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved				HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
Operation Type	RO				RW	RW	RW	RW
Default	0				0	0	0	0

Table 7.6.18 HB_CTRL_2 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5		
4		
3	HB6_HS_EN	0: HB6 high side disabled (default value) 1: HB6 high side enabled
2	HB6_LS_EN	0: HB6 low side disabled (default value) 1: HB6 low side enabled
1	HB5_HS_EN	0: HB5 high side disabled (default value) 1: HB5 high side enabled
0	HB5_LS_EN	0: HB5 low side disabled (default value) 1: HB5 low side enabled

Table 7.6.19 HB_PWM_CTRL1 register (REG_ADDR=0x0B)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB6_PWM_EN	HB5_PWM_EN	HB4_PWM_EN	HB3_PWM_EN	HB2_PWM_EN	HB1_PWM_EN
Operation Type	RO		RW	RW	RW	RW	RW	RW
Default	0		0	0	0	0	0	0

Table 7.6.20 HB_PWM_CTRL1 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5	HB6_PWM_EN	0: HB6 operate in SPI ON/OFF mode (default value) 1: HB6 operate in PWM mode
4	HB5_PWM_EN	0: HB5 operate in SPI ON/OFF mode (default value) 1: HB5 operate in PWM mode

3	HB4_PWM_EN	0: HB4 operate in SPI ON/OFF mode (default value) 1: HB4 operate in PWM mode
2	HB3_PWM_EN	0: HB3 operate in SPI ON/OFF mode (default value) 1: HB3 operate in PWM mode
1	HB2_PWM_EN	0: HB2 operate in SPI ON/OFF mode (default value) 1: HB2 operate in PWM mode
0	HB1_PWM_EN	0: HB1 operate in SPI ON/OFF mode (default value) 1: HB1 operate in PWM mode

Table 7.6.21 HB_PWM_CTRL2 register (REG_ADDR=0x0C)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		PWM6_DIS	PWM5_DIS	PWM4_DIS	PWM3_DIS	PWM2_DIS	PWM1_DIS
Operation Type	RO		RW	RW	RW	RW	RW	RW
Default	0		0	0	0	0	0	0

Table 7.6.22 HB_PWM_CTRL2 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5	PWM6_DIS	0: Internal PWM generator PWM6 enable (default value) 1: Internal PWM generator PWM6 disable
4	PWM5_DIS	0: Internal PWM generator PWM5 enable (default value) 1: Internal PWM generator PWM5 disable
3	PWM4_DIS	0: Internal PWM generator PWM4 enable (default value) 1: Internal PWM generator PWM4 disable
2	PWM3_DIS	0: Internal PWM generator PWM3 enable (default value) 1: Internal PWM generator PWM3 disable
1	PWM2_DIS	0: Internal PWM generator PWM2 enable (default value) 1: Internal PWM generator PWM2 disable
0	PWM1_DIS	0: Internal PWM generator PWM1 enable (default value) 1: Internal PWM generator PWM1 disable

Table 7.6.23 FW_CTRL_1 register (REG_ADDR=0x0D)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW
Operation Type	RO		RW	RW	RW	RW	RW	RW
Default	0		0	0	0	0	0	0

Table 7.6.24 FW_CTRL_1 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5	HB6_FW	0: HB6 operate in passive free-wheeling (default value) 1: HB6 operate in active free-wheeling
4	HB5_FW	0: HB5 operate in passive free-wheeling (default value) 1: HB5 operate in active free-wheeling
3	HB4_FW	0: HB4 operate in passive free-wheeling (default value) 1: HB4 operate in active free-wheeling

2	HB3_FW	0: HB3 operate in passive free-wheeling (default value) 1: HB3 operate in active free-wheeling
1	HB2_FW	0: HB2 operate in passive free-wheeling (default value) 1: HB2 operate in active free-wheeling
0	HB1_FW	0: HB1 operate in passive free-wheeling (default value) 1: HB1 operate in active free-wheeling

Table 7.6.25 PWM _MAP_CTRL_1 register (REG_ADDR=0x0F)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB2_PWM_MAP			HB1_PWM_MAP		
Operation Type	RW		RW			RW		
Default	00		000			000		

Table 7.6.26 PWM _MAP_CTRL_1 control register description

Bit	Field Name	Description
7	Reserved	Reserved, ‘00’ shall be used
6		
5	HB2_PWM_MAP	HB2 <-> internal PWM generator MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
4		
3		
2	HB1_PWM_MAP	HB1 <-> internal PWM generator MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
1		
0		

Table 7.6.27 PWM _MAP_CTRL_2 register (REG_ADDR=0x10)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB4_PWM_MAP			HB3_PWM_MAP		
Operation Type	RW		RW			RW		
Default	00		000			000		

Table 7.6.28 PWM _MAP_CTRL_2 control register description

Bit	Field Name	Description
7	Reserved	Reserved, ‘00’ shall be used
6		

5 4 3	HB4_PWM_MAP	HB4 <-> internal PWM generator MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
2 1 0	HB3_PWM_MAP	HB3 <-> internal PWM generator MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8

Table 7.6.29 PWM _MAP_CTRL_3 register (REG_ADDR=0x11)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB6_PWM_MAP			HB5_PWM_MAP		
Operation Type	RW		RW			RW		
Default	00		000			000		

Table 7.6.30 PWM _MAP_CTRL_3 control register description

Bit	Field Name	Description
7 6	Reserved	Reserved, ‘00’ shall be used
5 4 3	HB6_PWM_MAP	HB6 <-> internal PWM generator MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
2 1 0	HB5_PWM_MAP	HB5 <-> internal PWM generator MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8

Table 7.6.30 PWM _FREQ_CTRL_1 register (REG_ADDR=0x13)

	D7	D6	D5	D4	D3	D2	D1	D0

Field Name	PWM4_FREQ	PWM3_FREQ	PWM2_FREQ	PWM1_FREQ
Operation Type	RW	RW	RW	RW
Default	00	00	00	00

Table 7.6.31 PWM _FREQ_CTRL_1 control register Description

Bit	Field Name	Description
7 6	PWM4_FREQ	PWM4 typical frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
5 4	PWM3_FREQ	PWM3 typical frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
3 2	PWM2_FREQ	PWM2 typical frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
1 0	PWM1_FREQ	PWM1 typical frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz

Table 7.6.32 PWM _FREQ_CTRL_2 register (REG_ADDR=0x14)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved				PWM6_FREQ		PWM5_FREQ	
Operation Type	RO				RW		RW	
Default	00				00		00	

Table 7.6.33 PWM _FREQ_CTRL_2 control register description

Bit	Field Name	Description
7 6 5 4	Reserved	0: reversed (default value)
3 2	PWM6_FREQ	PWM6 typical frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
1	PWM5_FREQ	PWM5 typical frequency configuration 00: 80Hz (default value)

0		01: 100Hz 10: 200Hz 11: 2kHz

Table 7.6.34 PWM _DC_CTRL_1 register (REG_ADDR=0x15)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM1_DUTY_CYCLE							
Operation Type	RW							
Default	00000000							

Table 7.6.35 PWM _DC_CTRL_1 control register Description

Bit	Field Name	Description
7	PWM1_DUTY_CYCLE	PWM1 duty cycle calculation = 100% * BIT value /255
6		
5		
4		
3		
2		
1		
0		

Table 7.6.36 PWM _DC_CTRL_2 register (REG_ADDR=0x16)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM2_DUTY_CYCLE							
Operation Type	RW							
Default	00000000							

Table 7.6.37 PWM _DC_CTRL_2 control register description

Bit	Field Name	Description
7	PWM2_DUTY_CYCLE	PWM2 duty cycle calculation = 100% * BIT value /255
6		
5		
4		
3		
2		
1		
0		

Table 7.6.38 PWM _DC_CTRL_3 register (REG_ADDR=0x17)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM3_DUTY_CYCLE							

Operation Type	RW
Default	00000000

Table 7.6.39 PWM _DC_CTRL_3 control register description

Bit	Field Name	Description
7	PWM3_DUTY_CYCLE	PWM3 duty cycle calculation = 100% * BIT value /255
6		
5		
4		
3		
2		
1		
0		

Table 7.6.40 PWM _DC_CTRL_4 register (REG_ADDR=0x18)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM4_DUTY_CYCLE							
Operation Type	RW							
Default	00000000							

Table 7.6.41 PWM _DC_CTRL_4 control register description

Bit	Field Name	Description
7	PWM4_DUTY_CYCLE	PWM4 duty cycle calculation = 100% * BIT value /255
6		
5		
4		
3		
2		
1		
0		

Table 7.6.42 PWM _DC_CTRL_5 register (REG_ADDR=0x19)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM5_DUTY_CYCLE							
Operation Type	RW							
Default	00000000							

Table 7.6.43 PWM _DC_CTRL_5 control register description

Bit	Field Name	Description
7	PWM5_DUTY_CYCLE	PWM5 duty cycle calculation = 100% * BIT value /255
6		

5		
4		
3		
2		
1		
0		

Table 7.6.44 PWM _DC_CTRL_6 register (REG_ADDR=0x1A)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	PWM6_DUTY_CYCLE							
Operation Type	RW							
Default	00000000							

Table 7.6.45 PWM _DC_CTRL_6 control register description

Bit	Field Name	Description
7	PWM6_DUTY_CYCLE	PWM6 duty cycle calculation = 100% * BIT value /255
6		
5		
4		
3		
2		
1		
0		

Table 7.6.46 HB_SR_CTRL_1 Register (REG_ADDR=0x1D)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
Operation Type	RO		RW	RW	RW	RW	RW	RW
Default	0		0	0	0	0	0	0

Table 7.6.47 HB_SR_CTRL_1 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5	HB6_SR	0: HB6 power stage output rise / fall slew rate 0.6 V/us typ. (default value) 1: HB6 power stage output rise / fall slew rate 2.5 V/us typ.
4	HB5_SR	0: HB5 power stage output rise / fall slew rate 0.6 V/us typ. (default value) 1: HB5 power stage output rise / fall slew rate 2.5 V/us typ.
3	HB4_SR	0: HB4 power stage output rise / fall slew rate 0.6 V/us typ. (default value) 1: HB4 power stage output rise / fall slew rate 2.5 V/us typ.
2	HB3_SR	0: HB3 power stage output rise / fall slew rate 0.6 V/us typ. (default value) 1: HB3 power stage output rise / fall slew rate 2.5 V/us typ.
1	HB2_SR	0: HB2 power stage output rise / fall slew rate 0.6 V/us typ. (default value) 1: HB2 power stage output rise / fall slew rate 2.5 V/us typ.

0	HB1_SR	0: HB1 power stage output rise / fall slew rate 0.6 V/us typ. (default value) 1: HB1 power stage output rise / fall slew rate 2.5 V/us typ.

Table 7.6.48 OLP_CTRL_1 register (REG_ADDR=0x1F)

	D7 D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved	HB6_OPL_DIS	HB5_OPL_DIS	HB4_OPL_DIS	HB3_OPL_DIS	HB2_OPL_DIS	HB1_OPL_DIS
Operation Type	RO	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0

Table 7.6.49 OLP_CTRL_1 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5	HB6_OPL_DIS	0: HB6 active open load enable (default value) 1: HB6 active open load disable
4	HB5_OPL_DIS	0: HB5 active open load enable (default value) 1: HB5 active open load disable
3	HB4_OPL_DIS	0: HB4 active open load enable (default value) 1: HB4 active open load disable
2	HB3_OPL_DIS	0: HB3 active open load enable (default value) 1: HB3 active open load disable
1	HB2_OPL_DIS	0: HB2 active open load enable (default value) 1: HB2 active open load disable
0	HB1_OPL_DIS	0: HB8 active open load enable (default value) 1: HB8 active open load disable

Table 7.6.50 OLP_OC_CTRL_2 register (REG_ADDR=0x20)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	OPL_mask_FLT	OPL_HB_ACT	Reserved	OC_OFF_SR	Reserved			
Operation Type	RW	RW	RW	RW	RW			
Default	0	0	0	0	0000			

Table 7.6.51 OLP_OC_CTRL_2 control register description

Bit	Field Name	Description
7	OPL_mask_FLT	0: open load unmasked, reported on nfault (default value) 1: open load event is masked, not reported on nfault
6	OPL_HB_ACT	0: HB OFF, after OPL detected (default) 1: HB remains active, after OPL detected
5	Reserved	Reversed, ‘0’ shall be used
4	OC_OFF_SR	0: OCP event fast turn off slew rate (default value) 1: OCP event slow turn off slew rate
3	Reserved	Reserved, '0000' shall be used
2		
1		

0		

Table 7.6.52 OLP_OC_CTRL_3 register (REG_ADDR=0x21)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	OC_FILTER			Reserved				
Operation Type	RW			RW				
Default	000			00000				

Table 7.6.53 OLP_OC_CTRL_3 control register description

Bit	Field Name	Description
7 6 5	OC_FILTER	OCP typical deglitch filter timing 000: 10us (default value) 001: 5us 010: 2.5us 011: 1us 100: 60us 101: 40us 110: 30us 111: 20us
4 3 2 1 0	Reserved	Reserved, '00000' shall be used

Table 7.6.54 OLP_ CTRL_4 register (REG_ADDR=0x22)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB6_OPL_TH	HB5_OPL_TH	HB4_OPL_TH	HB3_OPL_TH	HB2_OPL_TH	HB1_OPL_TH
Operation Type	RO		RW	RW	RW	RW	RW	RW
Default	0		0	0	0	0	0	0

Table 7.6.55 OLP_ CTRL_4 control register description

Bit	Field Name	Description
7 6	Reserved	0: reversed (default value)
5	HB6_OPL_TH	0: HB6 active open load normal threshold and long open load filter used (default value) 1: HB6 active open load low threshold and short open load filter used
4	HB5_OPL_TH	0: HB5 active open load normal threshold and long open load filter used (default value) 1: HB5 active open load low threshold and short open load filter used
3	HB4_OPL_TH	0: HB4 active open load normal threshold and long open load filter used (default value) 1: HB4 active open load low threshold and short open load filter used
2	HB3_OPL_TH	0: HB3 active open load normal threshold and long open load filter used (default value) 1: HB3 active open load low threshold and short open load filter used
1	HB2_OPL_TH	0: HB2 active open load normal threshold and long open load filter used (default value) 1: HB2 active open load low threshold and short open load filter used

0	HB1_OPL_TH	0: HB1 active open load normal threshold and long open load filter used (default value) 1: HB1 active open load low threshold and short open load filter used

Table 7.6.56 GEN_ CTRL_1 register (REG_ADDR=0x25)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	SS_MOD		SS_DEV	RD_CLR_EN	unlock	SPI_ERR	Reversed	
Operation Type	RW		RW	RW	RW	RLR	RO	
Default	00		0	0	0	0	00	

Table 7.6.57 GEN_ CTRL_1 control register description

BIT	Field Name	Description
7 6	SS_MOD	spread spectrum configuration 00: disable spread spectrum (default value) 01: modulation freq 15.625 kHz 10: modulation freq 31.25 kHz 11: modulation freq 62.5 kHz
5	SS_DEV	0: modulation deviation 5% (typ） (default value) 1: modulation deviation 10% (typ）
4	RD_CLR_EN	0: SPI read command to clear diagnosis flag disable (default value) 1: SPI read command to clear diagnosis flag enable
3	unlock	0: OPL_CTRL_9 address 0x2E register bit 7~bit4 (OCPH_CONF, VM_OVPH_CONF, IDCH_CONF, TDEAD_MON_EN） 4 bits are in lock， write operation is ignored. (default value) 1. OPL_CTRL_9 address 0x2E register bit 7~bit4 (OCPH_CONF, VM_OVPH_CONF, IDCH_CONF, TDEAD_MON_EN） 4 bits are unlock， write operation is available. Note: Unlock function can temporarily allow user to change the 4 bits setting value. After power up, the 4 bits in OPL_CTRL_9 related with unlock function, are reset to default, and only determined by internal OTP.
2	SPI_ERR	0: No SPI communication error is detected. (default value). 1: An SPI communication error is detected.
1 0	Reversed	Reserved, '00' shall be used

Table 7.6.58 OLP_ CTRL_5 register (REG_ADDR=0x28)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	HB4_OFF_PU_EN	HB4_OFF_PD_EN	HB3_OFF_PU_EN	HB3_OFF_PD_EN	HB2_OFF_PU_EN	HB2_OFF_PD_EN	HB1_OFF_PU_EN	HB1_OFF_PD_EN
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Table 7.6.59 OPL_CTRL_5 control register description

Bit	Field Name	Description
7	HB4_OFF_PU_EN	0: HB4 off state open load pull up current disabled (default value) 1: HB4 off state open load pull up current enabled
6	HB4_OFF_PD_EN	0: HB4 off state open load pull down current disabled (default value) 1: HB4 off state open load pull down current enabled
5	HB3_OFF_PU_EN	0: HB3 off state open load pull up current disabled (default value) 1: HB3 off state open load pull up current enabled

4	HB3_OFF_PD_EN	0: HB3 off state open load pull down current disabled (default value) 1: HB3 off state open load pull down current enabled
3	HB2_OFF_PU_EN	0: HB2 off state open load pull up current disabled (default value) 1: HB2 off state open load pull up current enabled
2	HB2_OFF_PD_EN	0: HB2 off state open load pull down current disabled (default value) 1: HB2 off state open load pull down current enabled
1	HB1_OFF_PU_EN	0: HB1 off state open load pull up current disabled (default value) 1: HB1 off state open load pull up current enabled
0	HB1_OFF_PD_EN	0: HB1 off state open load pull down current disabled (default value) 1: HB1 off state open load pull down current enabled

Table 7.6.60 OLP_ CTRL_6 register (REG_ADDR=0x29)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved				HB6_OFF_PU_EN	HB6_OFF_PD_EN	HB5_OFF_PU_EN	HB5_OFF_PD_EN
Operation Type	RO				RW	RW	RW	RW
Default	0				0	0	0	0

Table 7.6.61 OLP_ CTRL_6 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5		
4		
3	HB6_OFF_PU_EN	0: HB6 off state open load pull up current disabled (default value) 1: HB6 off state open load pull up current enabled
2	HB6_OFF_PD_EN	0: HB6 off state open load pull down current disabled (default value) 1: HB6 off state open load pull down current enabled
1	HB5_OFF_PU_EN	0: HB5 off state open load pull up current disabled (default value) 1: HB5 off state open load pull up current enabled
0	HB5_OFF_PD_EN	0: HB5 off state open load pull down current disabled (default value) 1: HB5 off state open load pull down current enabled

Table 7.6.62 OLP_ CTRL_8 register (REG_ADDR=0x2D)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Reserved		HB6_IPUPD_MODE	HB5_IPUPD_MODE	HB4_IPUPD_MODE	HB3_IPUPD_MODE	HB2_IPUPD_MODE	HB1_IPUPD_MODE
Operation Type	RO		RW	RW	RW	RW	RW	RW
Default	0		0	0	0	0	0	0

Table 7.6.63 OLP_ CTRL_8 control register description

Bit	Field Name	Description
7	Reserved	0: reversed (default value)
6		
5	HB6_IPUPD_MODE	0: HB6 off diag fast charge current disable, low pull up / pull down current (default value) 1: HB6 off diag fast charge current enable, high pull up / pull down current
4	HB5_IPUPD_MODE	0: HB5 off diag fast charge current disable, low pull up / pull down current (default value) 1: HB5 off diag fast charge current enable, high pull up / pull down current

3	HB4_IPUPD_MODE	0: HB4 off diag fast charge current disable, low pull up / pull down current (default value) 1: HB4 off diag fast charge current enable, high pull up / pull down current
2	HB3_IPUPD_MODE	0: HB3 off diag fast charge current disable, low pull up / pull down current (default value) 1: HB3 off diag fast charge current enable, high pull up / pull down current
1	HB2_IPUPD_MODE	0: HB2 off diag fast charge current disable, low pull up / pull down current (default value) 1: HB2 off diag fast charge current enable, high pull up / pull down current
0	HB1_IPUPD_MODE	0: HB1 off diag fast charge current disable, low pull up / pull down current (default value) 1: HB1 off diag fast charge current enable, high pull up / pull down current

Table 7.6.64 OLP_ CTRL_9 register (REG_ADDR=0x2E)

	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	OCPH_CONF	VM_OVPH_CONF	IDCH_CONF	TDEAD_MON_EN	Reversed			
Operation Type	RW	RW	RW	RW	RW			
Default	0	0	0	1	0000			

Table 7.6.65 OLP_ CTRL_9 control register description

Bit	Field Name	Description
7	OCPH_CONF	0: OCP threshold typ 1.3A (default value) 1: OCP threshold typ 1.7A Note: It is not suggested to change OCP threshold setting, and default value after POR is determined by OTP
6	VM_OVPH_CONF	0: OVPH threshold typ 35v (default value) 1: OVPH threshold typ 37V Note: It is not suggested to change OVP threshold setting, and default value after POR is determined by OTP
5	IDCH_CONF	Configure HS and LS discharge pull down current level 0: pull down current level normal (default value) 1: pull down current level high Note: It is not suggested to change pull down current setting, default value after POR is determined by OTP
4	TDEAD_MON_EN	0: Tdead is determined by internal fixed timing 1: Tdead is determined by internal feedback signal (default value) Note: It is not suggested to change Tdead timing setting, default value after POR is determined by OTP
3	Reversed	Reserved, '0000' shall be used
2		
1		
0		

8. Application information

8.1. Application diagram

Figure 12. Typical application connection

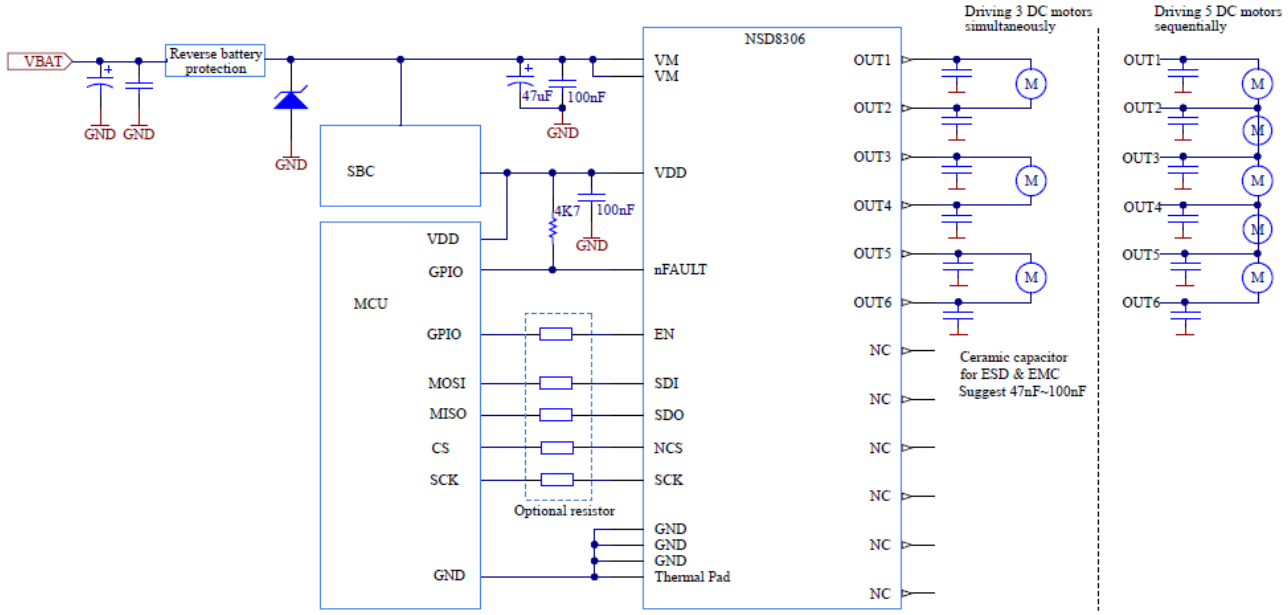
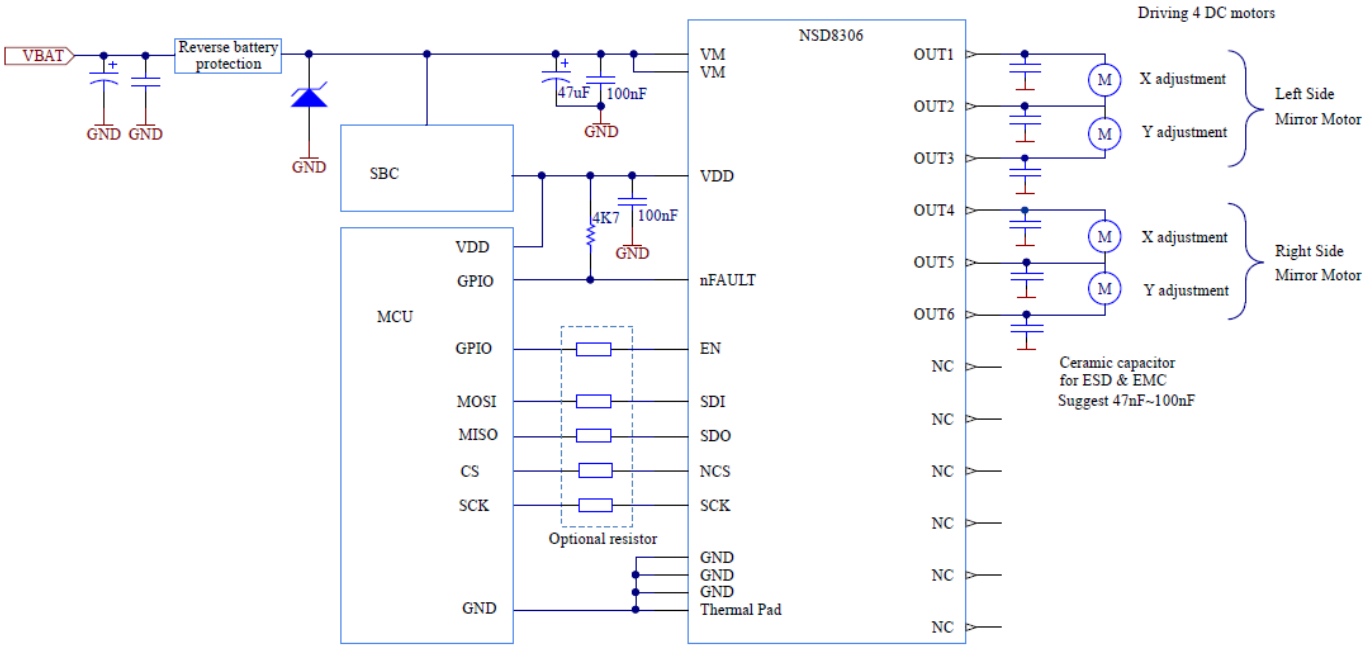
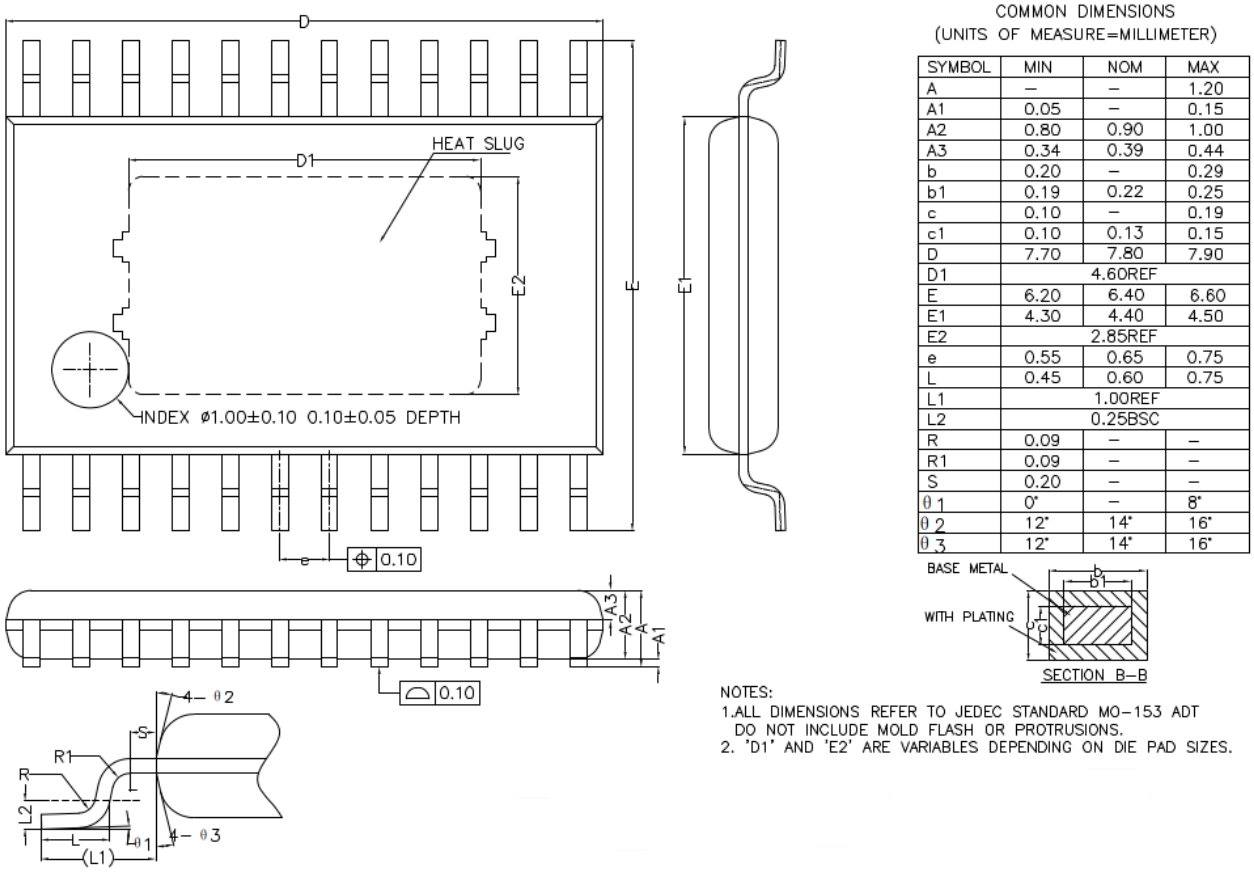


Figure 13. Typical application connection side mirror motor control



9. Package information

9.1. HTSSOP24 package information



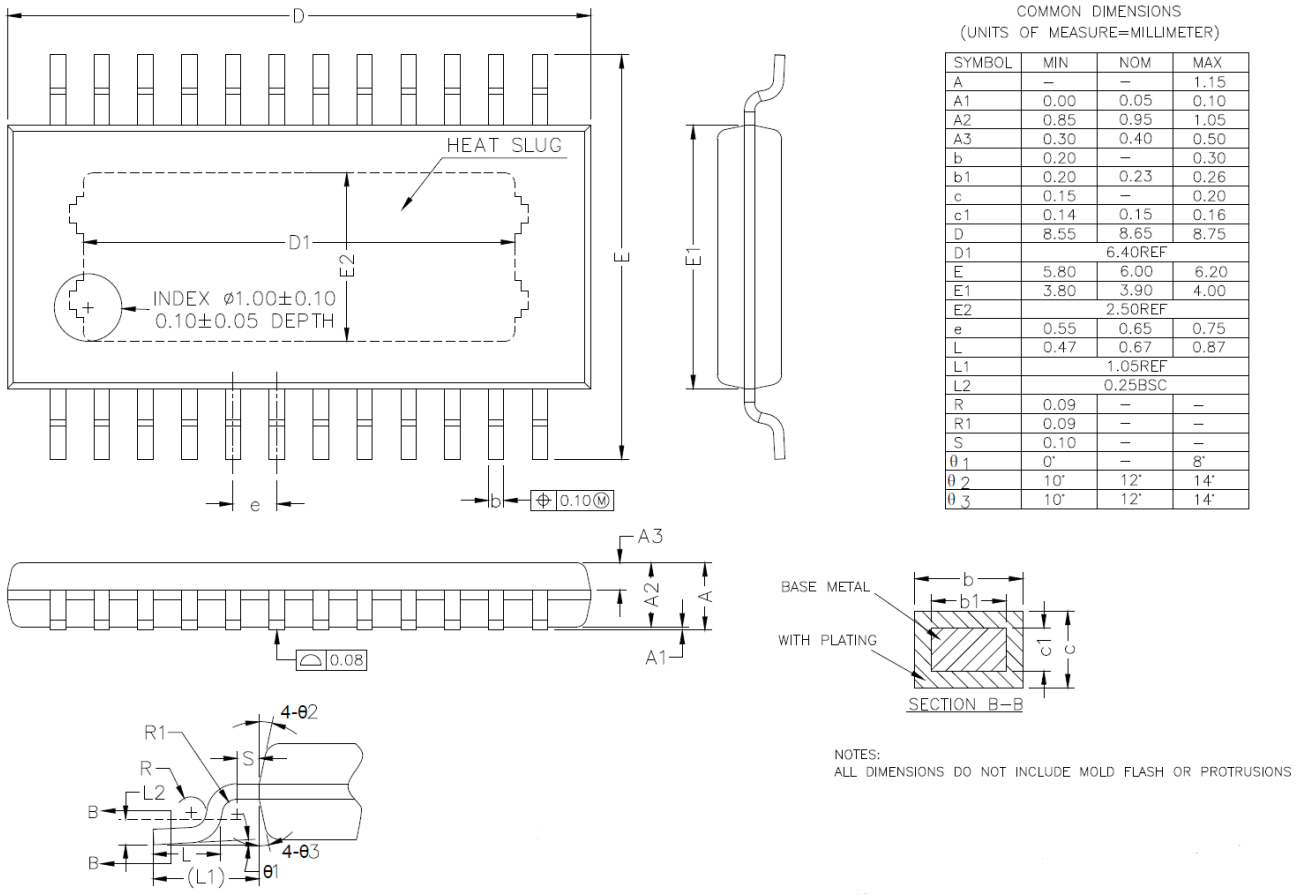
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	–	0.29
b1	0.19	0.22	0.25
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	7.70	7.80	7.90
D1		4.60REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.85REF	
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	12°	14°	16°
θ3	12°	14°	16°

NOTES:
1.ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 ADT
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. 'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

Figure 14. NSD8306 package information

9.2. HTSOP24 package information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.15
A1	0.00	0.05	0.10
A2	0.85	0.95	1.05
A3	0.30	0.40	0.50
b	0.20	–	0.30
b1	0.20	0.23	0.26
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	8.55	8.65	8.75
D1		6.40REF	
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2		2.50REF	
e	0.55	0.65	0.75
L	0.47	0.67	0.87
L1		1.05REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.10	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

Figure 15. NSD8306A package information

9.3. HTSSOP24 packaging information

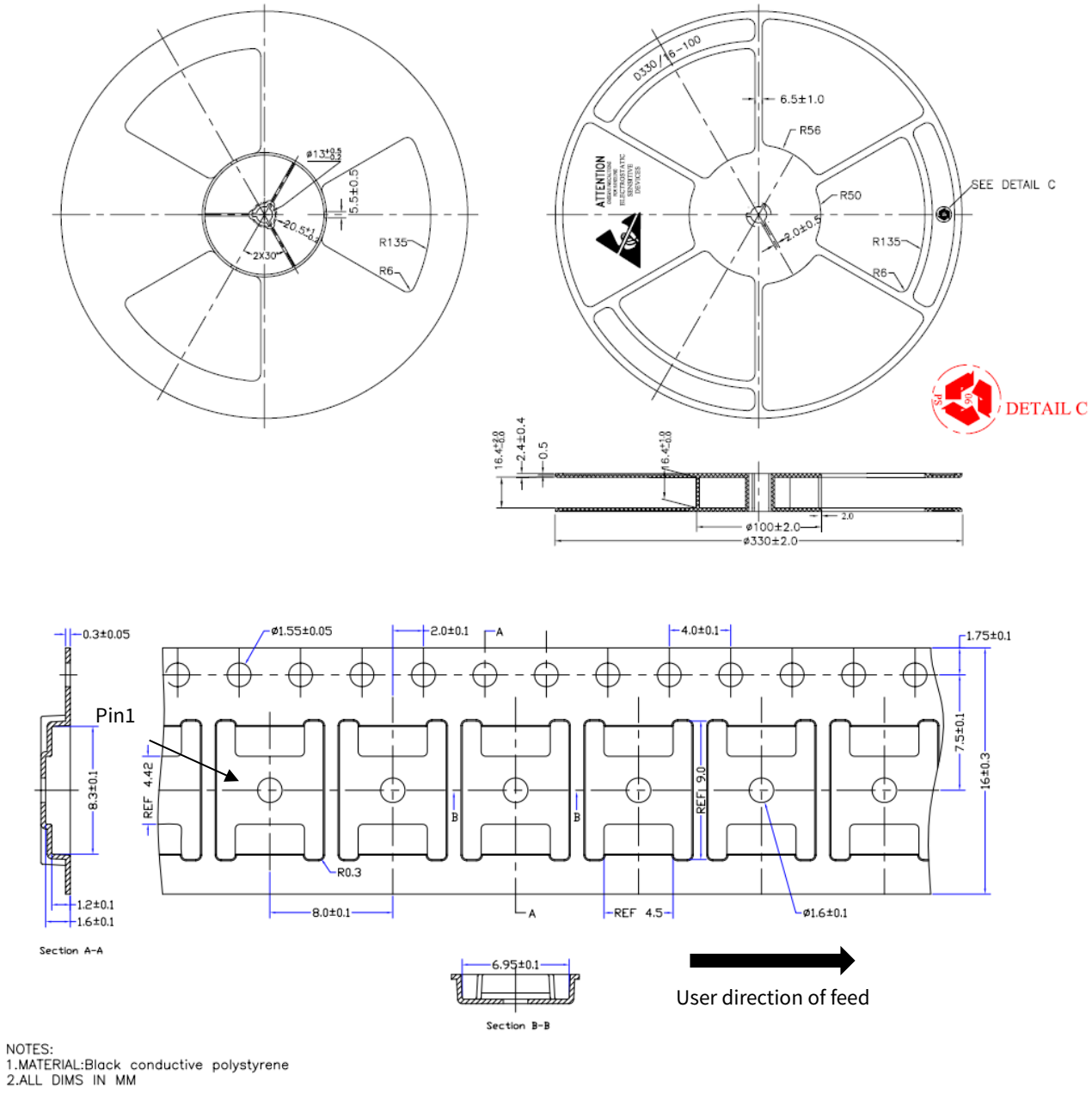


Figure 16. NSD8306 package information

9.4. HTSOP24 packaging information

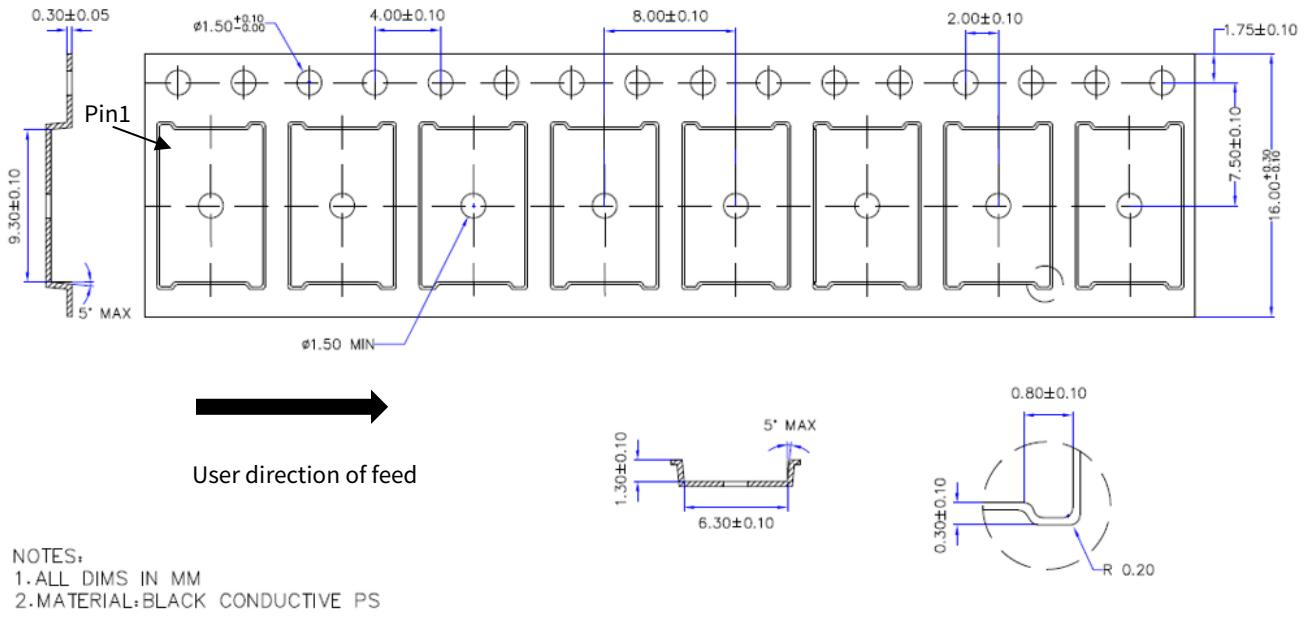


Figure 16. NSD8306A package information

10. Ordering Information

Part Number	*Package Type*	*MSL*	*SPQ*
NSD8306-Q1HTSXR	HTSSOP24	3	4000
NSD8306A-Q1HTSBR	HTSOP24	3	4000
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.			

11. Revision History

Revision	Description	Date
1.0	Initial version	2021/11/5
1.1	Adjust fonts and SPI register description format, insert SPI daisy chain description	2022/12/15
1.2	Revise some electrical characteristics and application example circuit	2023/03/22
1.3	Add package information of HTSOP24, revise some electrical parameters and register description	2023/07/18
1.4	Added pin description	2024/12/27

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