

Product Overview

The NSI822x devices are high reliability dual-channel digital isolators. The NSI822x device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms, 8kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI822x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSI822x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI822x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/us
- Chip level ESD: HBM: ±8kV
- Robust EMC Reinforced Dual-Channel Digital Isolators for SOW8 wide body and SOW16 wide body
- Default output high level or low level option
- Isolation surge voltage: >10kV
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -55°C~125°C
- RoHS-compliant packages:
 - SOP8 narrow body
 - SOW8 wide body
 - SOW16 wide body
 - SOWW16 wide body

Safety Regulatory Approvals

- UL recognition: up to 8000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

Part Number	Package	Body Size
NSI822xNx-DSPR	SOP8	4.90mm × 3.90mm
NSI822xWx-DSWVR	SOW8	5.85mm × 7.50mm
NSI822xWx-DSWR	SOW16	10.30mm × 7.50mm
NSI822xWx-DSWVR	SOWW16	10.52mm × 14.0mm

Functional Block Diagrams

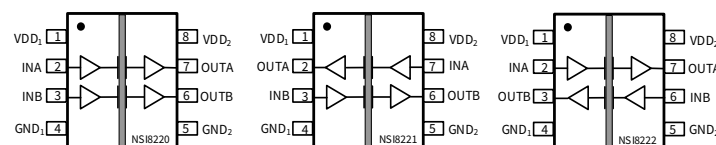


Figure 1. NSI822xNx SOP8 / NSI822xWx SOW8 Block Diagram

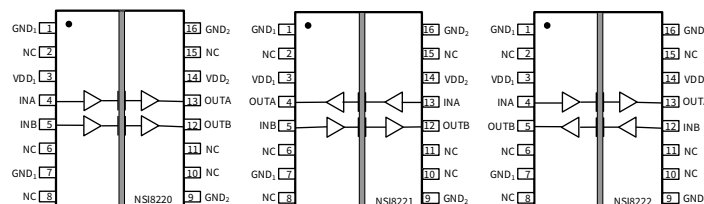


Figure 3. NSI822xWx SOW16 Block Diagram

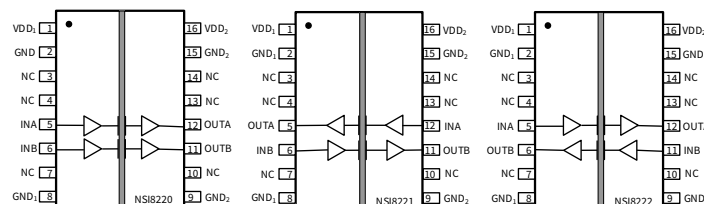


Figure 4. NSI822xWx SOWW16 Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS	9
3. RECOMMENDED OPERATING CONDITIONS	9
4. THERMAL CHARACTERISTICS	10
5. SPECIFICATIONS	10
5.1. ELECTRICAL CHARACTERISTICS	10
5.2. SUPPLY CURRENT CHARACTERISTICS – 5V SUPPLY	11
5.3. SUPPLY CURRENT CHARACTERISTICS –3.3V SUPPLY	12
5.4. SUPPLY CURRENT CHARACTERISTICS–2.5V SUPPLY	13
5.5. SWITCHING CHARACTERISTICS - 5V SUPPLY	14
5.6. SWITCHING CHARACTERISTICS - 3.3V SUPPLY	14
5.7. SWITCHING CHARACTERISTICS - 2.5V SUPPLY	15
5.8. TYPICAL PERFORMANCE CHARACTERISTICS	16
5.9. PARAMETER MEASUREMENT INFORMATION	17
6. HIGH VOLTAGE FEATURE DESCRIPTION	18
6.1. INSULATION AND SAFETY RELATED SPECIFICATIONS	18
6.2. INSULATION CHARACTERISTICS	18
6.3. SAFETY-LIMITING VALUES	20
6.4. REGULATORY INFORMATION	23
7. FUNCTION DESCRIPTION	25
7.1. OVERVIEW	25
7.2. OOK MODULATION	26
8. APPLICATION NOTE	27
8.1. TYPICAL APPLICATION CIRCUIT	27
8.2. PCB LAYOUT	27
8.3. HIGH SPEED PERFORMANCE	28
8.4. TYPICAL SUPPLY CURRENT EQUATIONS	28
9. PACKAGE INFORMATION	29
10. ORDER INFORMATION	33
11. DOCUMENTATION SUPPORT	34
12. TAPE AND REEL INFORMATION	35
13. REVISION HISTORY	40

1. Pin Configuration and Functions

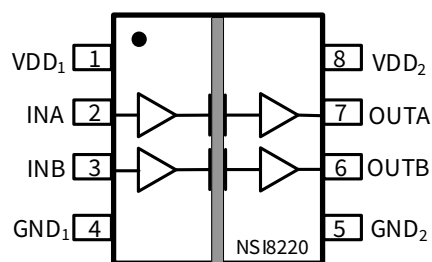


Figure 1.1 NSI8220N Package

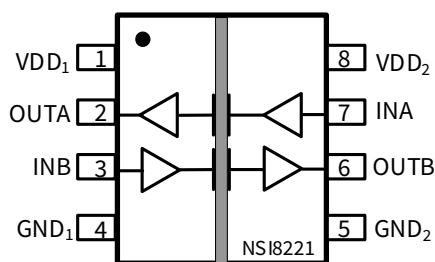


Figure 1.2 NSI8221N Package

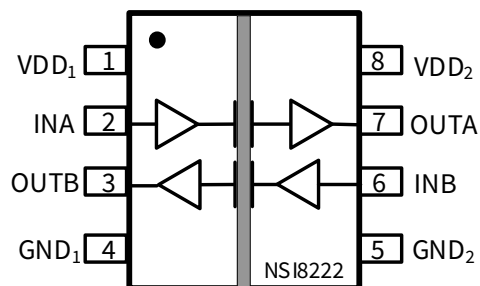


Figure 1.3 NSI8222N Package

Table 1.1 NSI8220N/ NSI8221N/ NSI8222N Pin Configuration and Description

NSI8220N PIN NO.	NSI8221N PIN NO.	NSI8222N PIN NO.	SYMBOL	FUNCTION
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

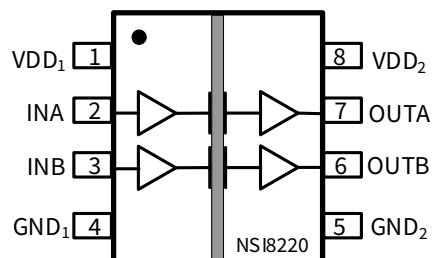


Figure 1.4 NSI8220Wx SOW8 Package

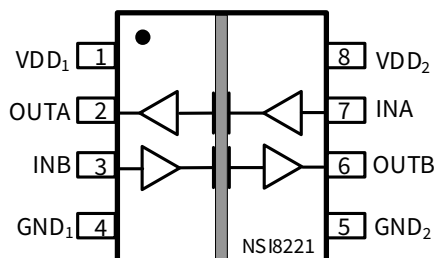


Figure 1.5 NSI8221Wx SOW8 Package

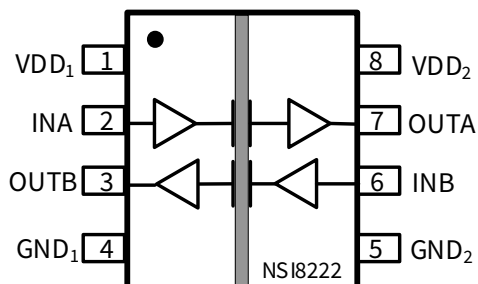


Figure 1.6 NSI8222Wx SOW8 Package

Table1.2 NSI8220W/ NSI8221W/ NSI8222W SOW8 Pin Configuration and Description

<i>NSI8220W</i> <i>SOW8</i> <i>PIN NO.</i>	<i>NSI8221W</i> <i>SOW8</i> <i>PIN NO.</i>	<i>NSI8222W</i> <i>SOW8</i> <i>PIN NO.</i>	<i>SYMBOL</i>	<i>FUNCTION</i>
1	1	1	VDD1	Power Supply for Isolator Side 1
2	7	2	INA	Logic Input A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
7	2	7	OUTA	Logic Output A
8	8	8	VDD2	Power Supply for Isolator Side 2

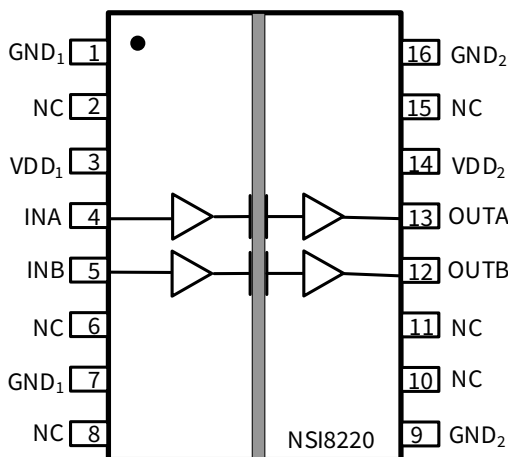


Figure 1.7 NSI8220W SOW16 Package

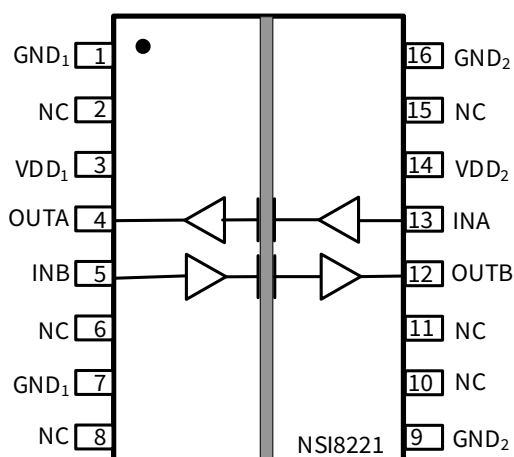


Figure 1.8 NSI8221W SOW16 Package

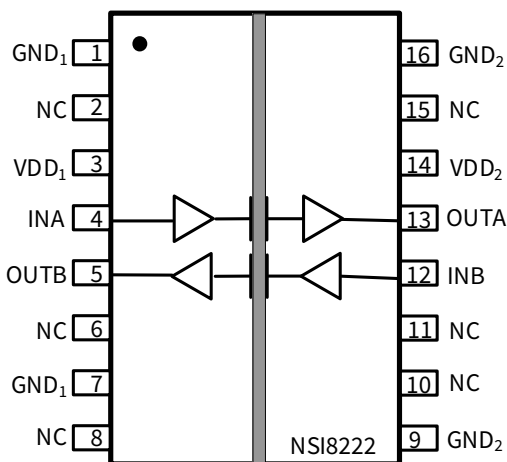


Figure 1.9 NSI8222W SOW16 Package

Table 1.3 NSI8220W/ NSI8221W/ NSI8222W SOW16 Pin Configuration and Description

NSI8220W SOW16 PIN NO.	NSI8221W SOW16 PIN NO.	NSI8222W SOW16 PIN NO.	SYMBOL	FUNCTION
1	1	1	GND1	Ground 1, the ground reference for Isolator Side 1
2	2	2	NC	No Connection.
3	3	3	VDD1	Power Supply for Isolator Side 1
4	13	4	INA	Logic Input A
5	5	12	INB	Logic Input B
6	6	6	NC	No Connection.
7	7	7	GND1	Ground 1, the ground reference for Isolator Side 1

NSI8220W SOW16 PIN NO.	NSI8221W SOW16 PIN NO.	NSI8222W SOW16 PIN NO.	SYMBOL	FUNCTION
8	8	8	NC	No Connection.
9	9	9	GND2	Ground 2, the ground reference for Isolator Side 2
10	10	10	NC	No Connection.
11	11	11	NC	No Connection.
12	12	5	OUTB	Logic Output B
13	4	13	OUTA	Logic Output A
14	14	14	VDD2	Power Supply for Isolator Side 2
15	15	15	NC	No Connection.
16	16	16	GND2	Ground 2, the ground reference for Isolator Side 2

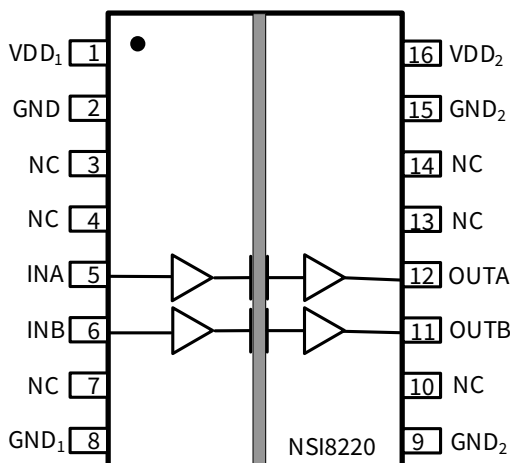


Figure 1.10 NSI8220W SOWW16 Package

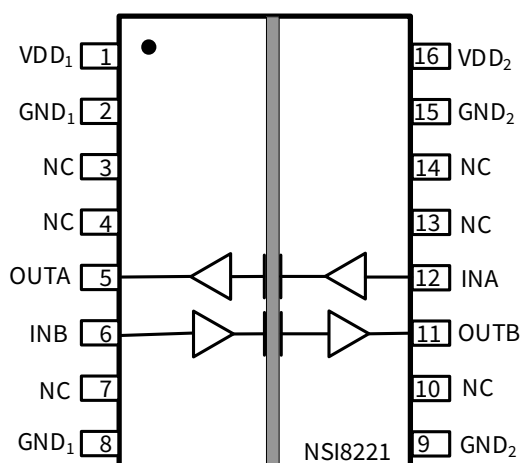


Figure 1.11 NSI8221W SOWW16 Package

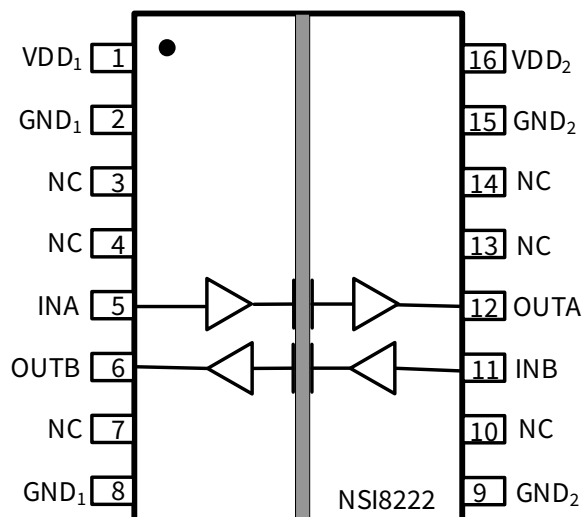


Figure 1.12 NSI8222W SOWW16 Package

Table 1.4 NSI8220W/ NSI8221W/ NSI8222W SOWW16 Pin Configuration and Description

NSI8220W SOWW16 PIN NO.	NSI8221W SOWW16 PIN NO.	NSI8222W SOWW16 PIN NO.	SYMBOL	FUNCTION
1	1	1	VDD1	Power Supply for Isolator Side 1
2	2	2	GND1	Ground 1, the ground reference for Isolator Side 1
3	3	3	NC	No Connection.
4	4	4	NC	No Connection.
5	12	5	INA	Logic Input A
6	6	11	INB	Logic Input B
7	7	7	NC	No Connection.

NSI8220W SOWW16 PIN NO.	NSI8221W SOWW16 PIN NO.	NSI8222W SOWW16 PIN NO.	SYMBOL	FUNCTION
8	8	8	GND1	Ground 1, the ground reference for Isolator Side 1
9	9	9	GND2	Ground 2, the ground reference for Isolator Side 2
10	10	10	NC	No Connection.
11	11	6	OUTB	Logic Output B
12	5	12	OUTA	Logic Output A
13	13	13	NC	No Connection.
14	14	14	NC	No Connection.
15	15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	16	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	V _{INA} , V _{INB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	V _{OUTA} , V _{OUTB}	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	V _{INA} , V _{INB} , V _{OUTA} , V _{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	I _o	-15		15	mA	
Operating Temperature	T _{opr}	-55		125	°C	
Junction Temperature	T _j			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	min	typ	max	unit
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T _{opr}	-55		125	°C
High Level Input Voltage	V _{IH}	2			V
Low Level Input Voltage	V _{IL}			0.8	V
Data rate	DR			150	Mbps

4. Thermal Characteristics

Parameters	Symbol	SOWW16	SOW16	SOW8	SOP8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	86.5	86.5	84.3	137.7	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	49.6	49.6	36.3	54.9	°C/W
Junction-to-board thermal resistance	θ_{JB}	49.7	49.7	47.0	71.7	°C/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR}	2	2.2	2.4	V	POR threshold as during power-up
	VDD _{HYS}		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V _{IT+}		1.6	2	V	
Falling input switching threshold	V _{IT-}	0.8	1.2		V	
Input threshold voltage hysteresis	V _{I(HYS)}		0.4		V	
High Level Output Voltage	V _{OH}	VDD-0.4			V	I _{OH} ≤ 4mA
Low Level Output Voltage	V _{OL}			0.4	V	I _{OL} ≤ 4mA
Output Impedance	R _{out}		50		ohm	
Input Pull high or low Current	I _{pull}		8	15	uA	
Start Up Time after POR	tr _{bs}		10		usec	
Common Mode Transient Immunity	CMTI	±200	±250		kV/us	See Figure 5.8

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8220					
	I _{DD1} (Q0)		0.59	0.89	mA	All Input 0V for NSI8220x0 Or All Input at supply for NSI8220x1
	I _{DD2} (Q0)		1.29	1.94	mA	
	I _{DD1} (Q1)		2.80	4.20	mA	All Input at supply for NSI8220x0 Or All Input 0V for NSI8220x1
	I _{DD2} (Q1)		1.32	1.98	mA	
	I _{DD1} (1M)		1.70	2.55	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.39	2.09	mA	
	I _{DD1} (10M)		1.78	2.67	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		2.13	3.20	mA	
	I _{DD1} (100M)		2.49	4.23	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		9.22	15.66	mA	
	NSI8221/ NSI8222					
	I _{DD1} (Q0)		0.94	1.41	mA	All Input 0V for NSI822xx0 Or All Input at supply for NSI822xx1
	I _{DD2} (Q0)		0.94	1.41	mA	
	I _{DD1} (Q1)		2.06	3.09	mA	All Input at supply for NSI822xx0 Or All Input 0V for NSI822xx1
	I _{DD2} (Q1)		2.06	3.09	mA	
	I _{DD1} (1M)		1.55	2.32	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		1.55	2.32	mA	
	I _{DD1} (10M)		1.96	2.93	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		1.96	2.93	mA	
	I _{DD1} (100M)		5.86	10.05	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		5.86	10.05	mA	

5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8220					
	I _{DD1} (Q0)		0.56	0.83	mA	All Input 0V for NSI8220x0 Or All Input at supply for NSI8220x1
	I _{DD2} (Q0)		1.24	1.86	mA	
	I _{DD1} (Q1)		2.76	4.13	mA	All Input at supply for NSI8220x0 Or All Input 0V for NSI8220x1
	I _{DD2} (Q1)		1.27	1.91	mA	
	I _{DD1} (1M)		1.66	2.49	mA	All Input with 1Mbps, C _L = 15pF
	I _{DD2} (1M)		1.31	1.97	mA	
	I _{DD1} (10M)		1.71	2.57	mA	All Input with 10Mbps, C _L = 15pF
	I _{DD2} (10M)		1.80	2.70	mA	
	I _{DD1} (100M)		2.20	3.65	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		6.50	10.77	mA	
	NSI8221/ NSI8222					
	I _{DD1} (Q0)		0.90	1.35	mA	All Input 0V for NSI822xx0 Or All Input at supply for NSI822xx1
	I _{DD2} (Q0)		0.90	1.35	mA	
	I _{DD1} (Q1)		2.01	3.02	mA	All Input at supply for NSI822xx0 Or All Input 0V for NSI822xx1
	I _{DD2} (Q1)		2.01	3.02	mA	
	I _{DD1} (1M)		1.49	2.23	mA	All Input with 1Mbps, C _L = 15pF
	I _{DD2} (1M)		1.49	2.23	mA	
	I _{DD1} (10M)		1.76	2.63	mA	All Input with 10Mbps, C _L = 15pF
	I _{DD2} (10M)		1.76	2.63	mA	
	I _{DD1} (100M)		4.35	7.27	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		4.35	7.27	mA	

5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8220					
	I _{DD1} (Q0)		0.54	0.81	mA	All Input 0V for NSI8220x0 Or All Input at supply for NSI8220x1
	I _{DD2} (Q0)		1.22	1.83	mA	
	I _{DD1} (Q1)		2.73	4.10	mA	All Input at supply for NSI8220x0 Or All Input 0V for NSI8220x1
	I _{DD2} (Q1)		1.24	1.86	mA	
	I _{DD1} (1M)		1.64	2.46	mA	All Input with 1Mbps, C _L = 15pF
	I _{DD2} (1M)		1.27	1.91	mA	
	I _{DD1} (10M)		1.67	2.51	mA	All Input with 10Mbps, C _L = 15pF
	I _{DD2} (10M)		1.65	2.48	mA	
	I _{DD1} (100M)		1.98	3.23	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		5.22	8.53	mA	
	NSI8221/ NSI8222					
	I _{DD1} (Q0)		0.88	1.32	mA	All Input 0V for NSI822xx0 Or All Input at supply for NSI822xx1
	I _{DD2} (Q0)		0.88	1.32	mA	
	I _{DD1} (Q1)		1.99	2.98	mA	All Input at supply for NSI822xx0 Or All Input 0V for NSI822xx1
	I _{DD2} (Q1)		1.99	2.98	mA	
	I _{DD1} (1M)		1.46	2.18	mA	All Input with 1Mbps, C _L = 15pF
	I _{DD2} (1M)		1.46	2.18	mA	
	I _{DD1} (10M)		1.66	2.49	mA	All Input with 10Mbps, C _L = 15pF
	I _{DD2} (10M)		1.66	2.49	mA	
	I _{DD1} (100M)		3.60	5.93	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		3.60	5.93	mA	

5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}	2.5	6.54	15	ns	See Figure 5.7 , C _L = 15pF
	t _{PHL}	2.5	8.30	15	ns	See Figure 5.7 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 5.7 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 5.7 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 5.7 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT} (PK)		350		ps	
Channel-to-Channel Delay Skew	t _{SK} (c2c)			2.5	ns	
Part-to-Part Delay Skew	t _{SK} (p2p)			5.0	ns	

5.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V**, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}	2.5	8.0	15	ns	See Figure 5.7 , C _L = 15pF
	t _{PHL}	2.5	8.7	15	ns	See Figure 5.7 , C _L = 15pF
Pulse Width Distortion t _{PHL} - t _{PLH}	PWD			5.0	ns	See Figure 5.7 , C _L = 15pF
Rising Time	t _r			5.0	ns	See Figure 5.7 , C _L = 15pF
Falling Time	t _f			5.0	ns	See Figure 5.7 , C _L = 15pF
Peak Eye Diagram Jitter	t _{JIT} (PK)		350		ps	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

5.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.7 , $C_L = 15pF$
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.7 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 5.7 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 5.7 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 5.7 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

5.8. Typical Performance Characteristics

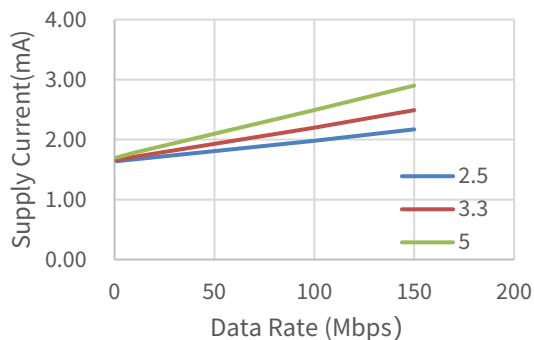


Figure 5.1 NSI8220 VDD1 Supply Current vs Data Rate

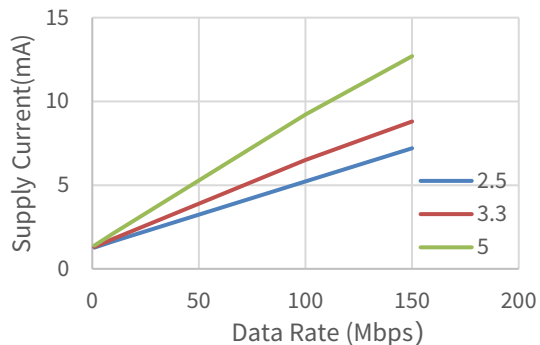


Figure 5.2 NSI8220 VDD2 Supply Current vs Data Rate

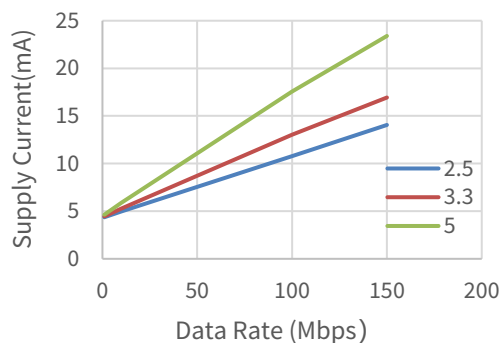


Figure 5.3 NSI8221/ NSI8222 VDD1 Supply Current vs Data Rate

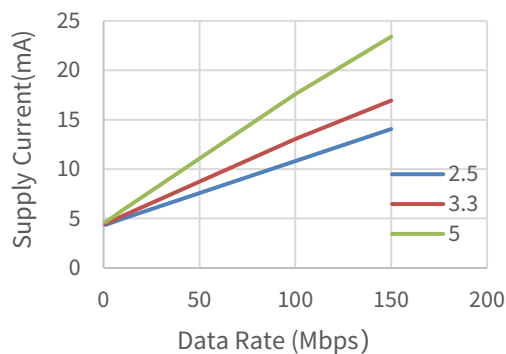


Figure 5.4 NSI8221/ NSI8222 VDD2 Supply Current vs Data Rate

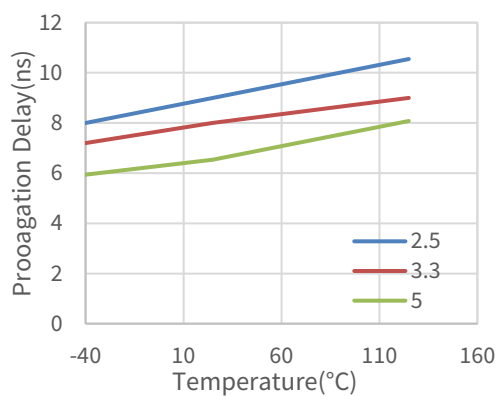


Figure 5.5 Rising Edge Propagation Delay Vs Temp

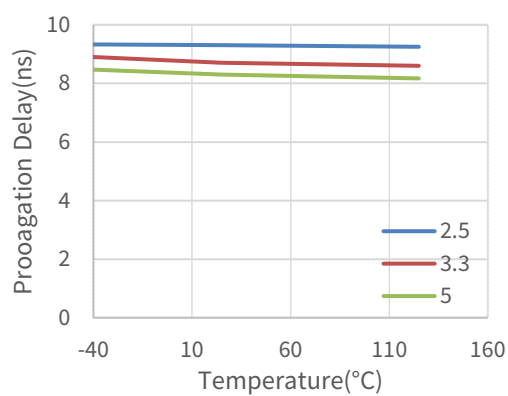
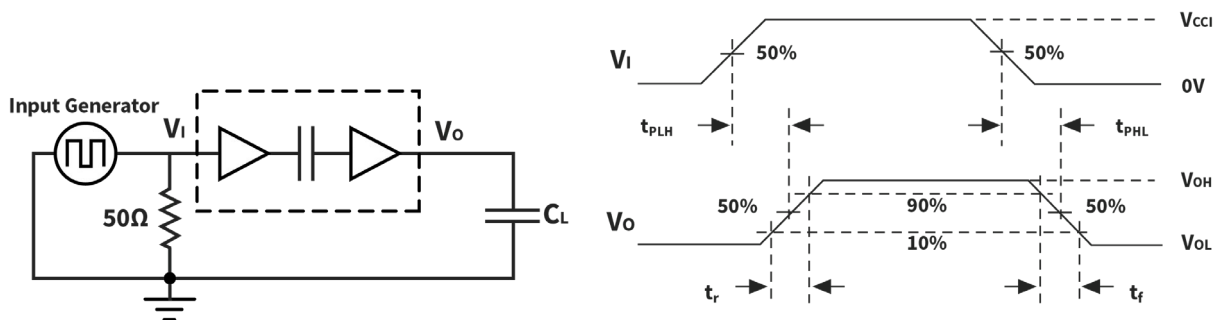


Figure 5.6 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information



(1) Input Generator Characteristics : $PRR \leq 50\text{kHz}$, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, Duty cycle = 50%, $Z_o = 50\ \Omega$.

Figure 5.7 Switching Characteristics Test Circuit and Waveform

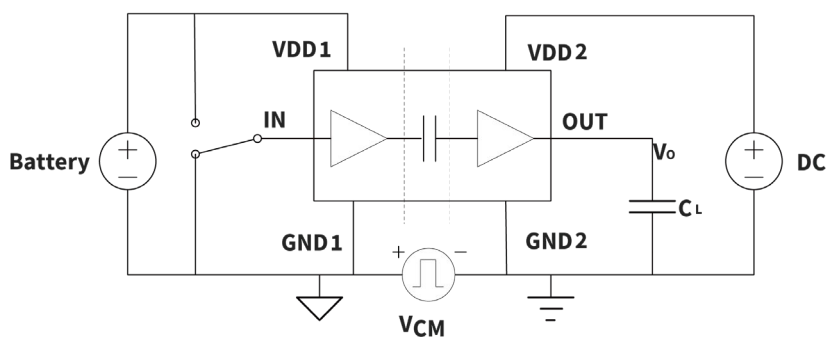


Figure 5.8 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value				Unit	Comments
		SOP8	SOW8	SOW16	SOWW16		
Minimum External Clearance	CLR	4.0	8.0	8.0	15	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	4.0	8.0	8.0	15	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28				um	
Tracking Resistance (Comparative Tracking Index)	CTI	>600	>600	>600	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I	I	I	I		IEC 60664-1

Description	Test Condition	Value			
		SOP8	SOW8	SOW16	SOWW16
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq$ 150Vrms	I to IV	I to IV	I to IV	I to IV
	For Rated Mains Voltage $\leq$ 300Vrms	I to III	I to IV	I to IV	I to IV
	For Rated Mains Voltage $\leq$ 600Vrms	I to II	I to IV	I to IV	I to IV
	For Rated Mains Voltage $\leq$ 1000Vrms	I	I to III	I to III	I to III
Climatic Classification		40/125/21			
Pollution Degree per DIN VDE 0110,		2			

6.2. Insulation Characteristics

Description	Test Condition	Symbol	Value				Unit
			SOP8	SOW8	SOW16	SOWW16	
Maximum repetitive isolation voltage		V_{IORM}	565	2121	2121	2121	V_{PEAK}
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	1500	1500	1500	V_{RMS}
	DC voltage		565	2121	2121	2121	V_{DC}

Description	Test Condition	Symbol	Value				Unit
			SOP8	SOW8	SOW16	SOWW16	
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.2 \cdot V_{IORM}$, $t_m=10\text{ s}$.	q_{pd}					pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.6 \cdot V_{IORM}$, $t_m=10\text{ s}$			<5	<5	<5	pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2 \cdot V_{IOTM}$, $t_{ini}=1\text{ s}$ $V_{pd(m)}=1.875 \cdot V_{IORM}$, $t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)						pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.2 \cdot V_{IORM}$, $t_m=10\text{ s}$.	q_{pd}	<5				pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.3 \cdot V_{IORM}$, $t_m=10\text{ s}$						pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2 \cdot V_{IOTM}$, $t_{ini}=1\text{ s}$ $V_{pd(m)}=1.5 \cdot V_{IORM}$, $t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)						pC
Maximum transient isolation voltage	$t=60\text{ sec}$	V_{IOTM}	5300	8000	8000	12000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	5384	6250	6250	8000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	7000	10000	10000	12800	V_{PEAK}
Isolation resistance	$V_{IO}=500\text{ V}$, $T_{amb}=25^\circ\text{C}$	R_{IO}	$>10^{12}$	$>10^{12}$	$>10^{12}$	$>10^{12}$	Ω

Description	Test Condition	Symbol	Value				Unit
			SOP8	SOW8	SOW16	SOWW16	
	$V_{IO} = 500V, 100^{\circ}C \leq T_{amb} \leq 125^{\circ}C$		$>10^{11}$	$>10^{11}$	$>10^{11}$	$>10^{11}$	Ω
	$V_{IO} = 500V, T_{amb} = T_s$		$>10^9$	$>10^9$	$>10^9$	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	0.6	0.6	0.6	0.6	pF
UL1577							
Withstand Isolation Voltage	$V_{TEST} = V_{ISO}, t = 60 s$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}, t = 1 s$ (100% production test)	V_{ISO}	3750	5000	5000	8500	V_{RMS}

6.3. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-17 of NSI822xN-DSPR SOP8(150mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 137.7^{\circ}C/W, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	908	mW
Safety Supply Current	$R_{\theta JA} = 137.7^{\circ}C/W, V_I = 5.5 V, T_J = 150^{\circ}C, T_A = 25^{\circ}C$	165	mA
Safety Temperature ²⁾		150	$^{\circ}C$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8(150mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

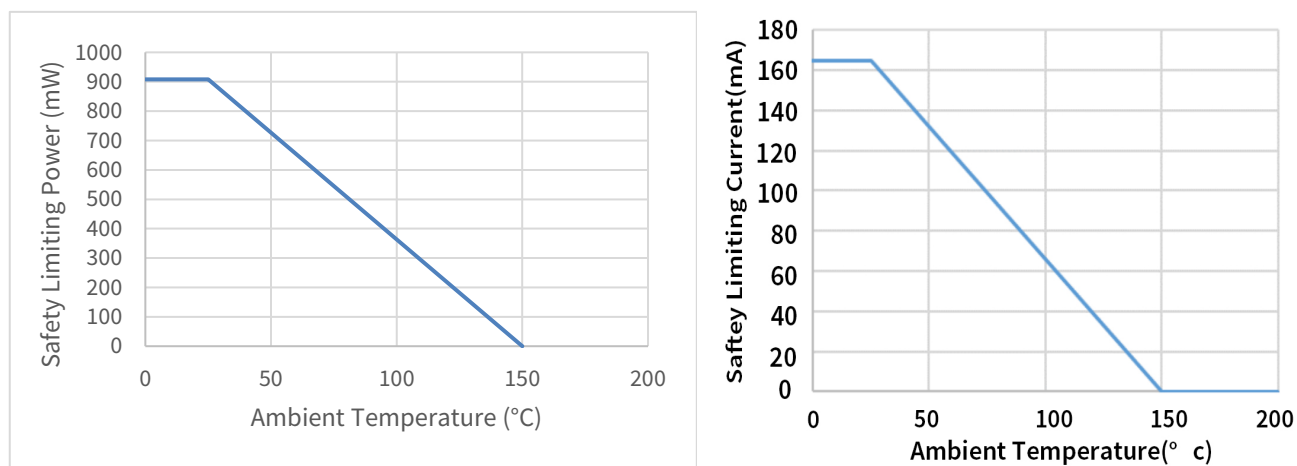


Figure 6.1 NSI822xN-DSPR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI822xW-DSWVR SOW8(300mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 84.3 \text{ }^{\circ}\text{C/W}$, $V_I = 5.5 \text{ V}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$	1483	mW
Safety Supply Current	$R_{\theta JA} = 84.3 \text{ }^{\circ}\text{C/W}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$	269.6	mA
Safety Temperature ²⁾		150	$^{\circ}\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW8(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

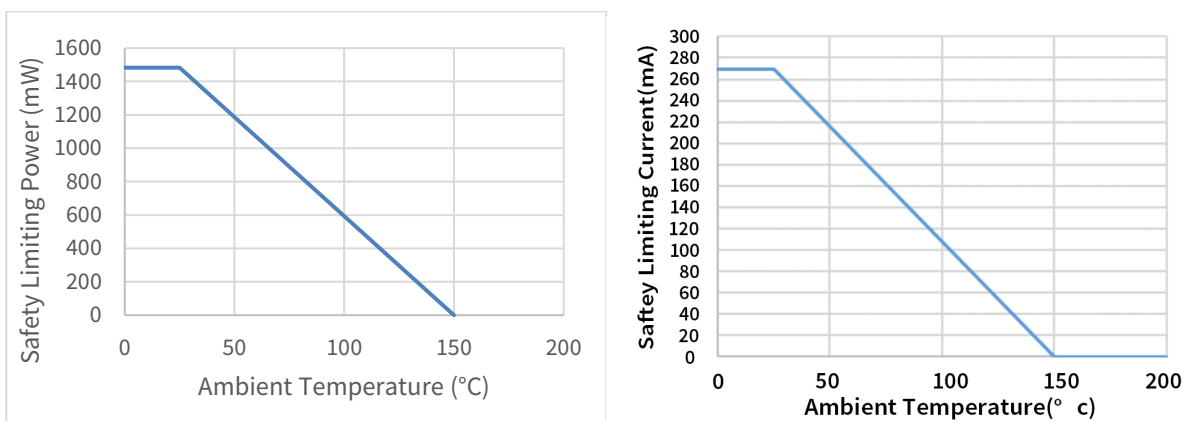


Figure 6.2 NSI822xW-DSWVR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI822xW-DSWR SOW16(300mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 86.5 \text{ }^{\circ}\text{C/W}$, $V_I = 5.5 \text{ V}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$	1445	mW
Safety Supply Current	$R_{\theta JA} = 86.5 \text{ }^{\circ}\text{C/W}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$	262.7	mA
Safety Temperature ²⁾		150	$^{\circ}\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

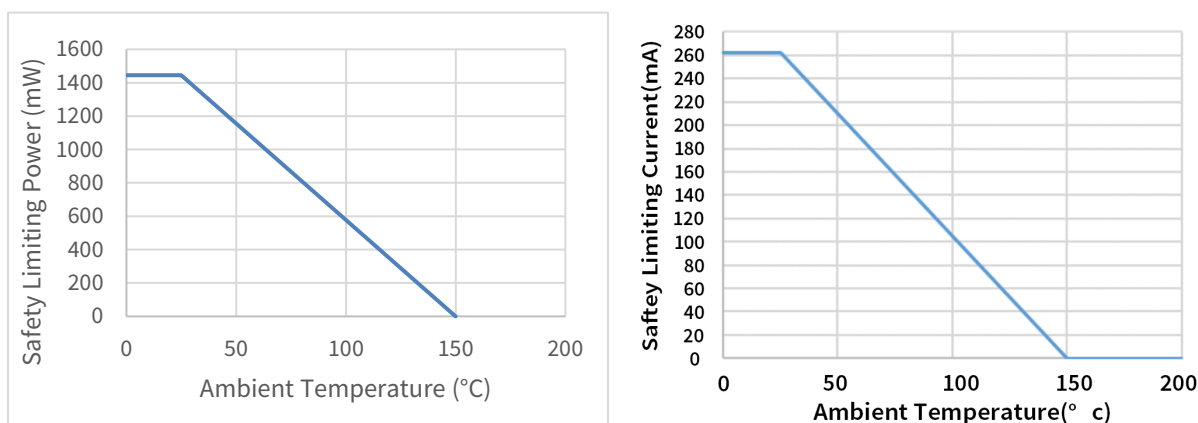


Figure 6.3 NSI822xW-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI822xW-DSWWR SOWW16(600mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 86.5 \text{ }^{\circ}\text{C/W}$, $V_I = 5.5 \text{ V}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$	1445	mW
Safety Supply Current	$R_{\theta JA} = 86.5 \text{ }^{\circ}\text{C/W}$, $T_J = 150 \text{ }^{\circ}\text{C}$, $T_A = 25 \text{ }^{\circ}\text{C}$	262.7	mA
Safety Temperature ²⁾		150	$^{\circ}\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOWW16(600mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

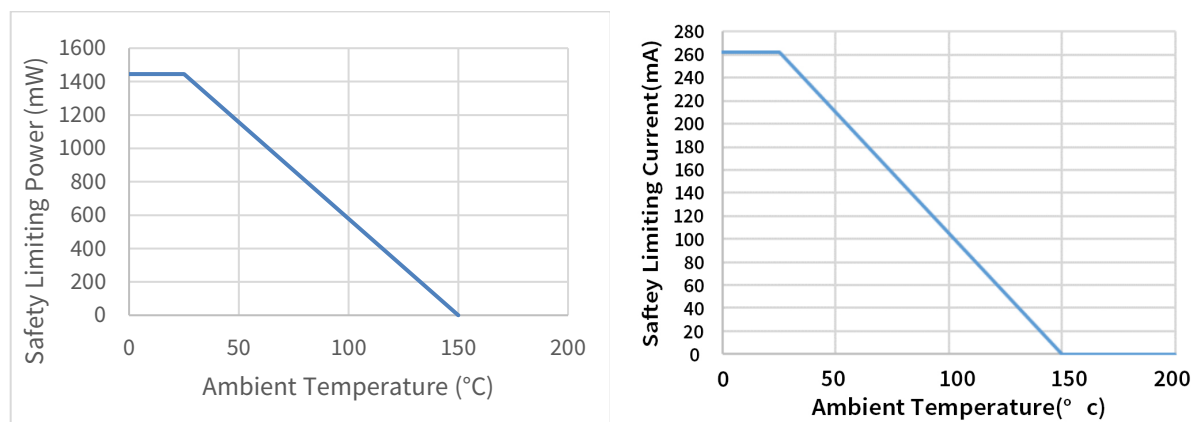


Figure 6.4 NSI822xW-DSWWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17

6.4. Regulatory Information

The NSI822xN-DSPP are approved by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 3750V _{rms} Isolation voltage	Single Protection, 3750V _{rms} Isolation voltage	Basic Insulation V _{IORM} =565V _{peak} V _{IOTM} =5300V _{peak} V _{IOSM} =7000V _{peak}	Basic insulation	3000Vrms for 1min
E500602	E500602	40050121	CQC20001264940	R50574061

The NSI822xW-DSWVR are approved by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264938	R50574061

The NSI822xW-DSWR are approved by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000Vrms for 1min
E500602	E500602	40052820	CQC20001264939	R50574061

The NSI822xW-DSWWR are approved by the organizations listed in table.

CUL		VDE	CQC	TUV
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 8000V _{rms} Isolation voltage	Single Protection, 8000V _{rms} Isolation voltage	Reinforced Insulation V _{IORM} =2121V _{peak} V _{IOTM} =12000V _{peak} V _{IOSM} =12800V _{peak}	Reinforced insulation	5000V _{rms} for 1min
E500602	E500602	40052820	CQC23001379406	R50574061

7. Function Description

7.1. Overview

The NSI822x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI822x devices are high reliability dual-channel digital isolator. The NSI822x device is safety certified by UL1577 support several insulation withstand voltages (3.75kV_{rms}, 5kV_{rms}), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI822x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSI822x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI822x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI822x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60us after powering up.

Table 7.1 Output status vs. power status

Input ¹	VDDIN status	VDDOUT status	Output	Comment
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI822xx0) H(NSI822xx1)	The output follows the same status with the input within 60us after input side VDD is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input within 60us after output side VDD is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDDIN is input side power; VDDOUT is output side power. (1) There is a protection diode between the input and the VDDIN. When the VDDIN is floating, the strong drive signal through the input pin will put the VDDIN in an indeterminate state.				

7.2. OOK Modulation

NSI822x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

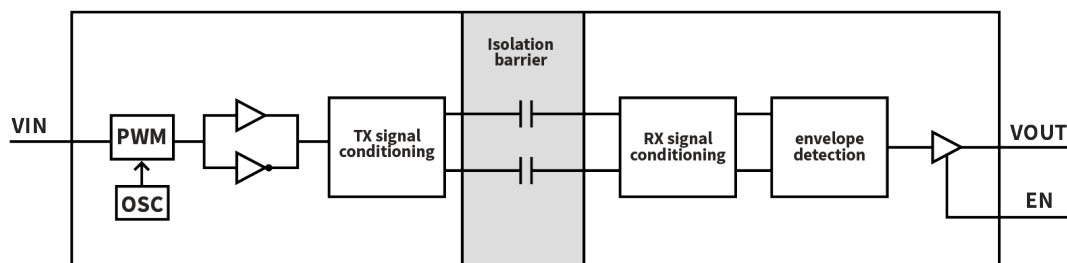


Figure 7.1 Single Channel Function Block Diagram

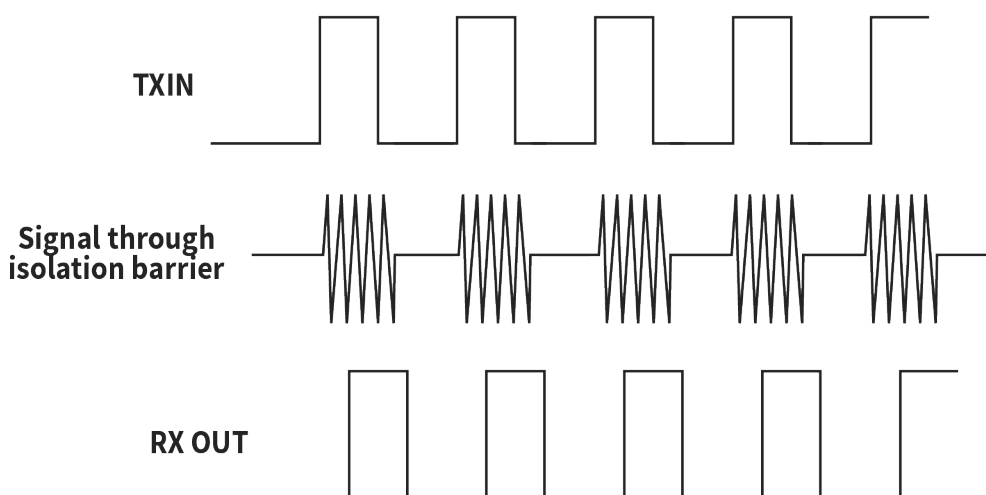


Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

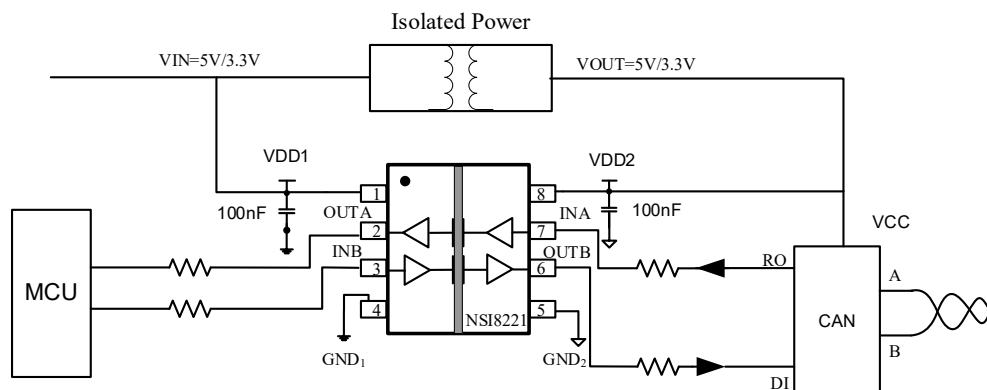


Figure 8.1 Typical SCH for ISO CAN Interface

8.2. PCB Layout

The NSI822x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.5 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

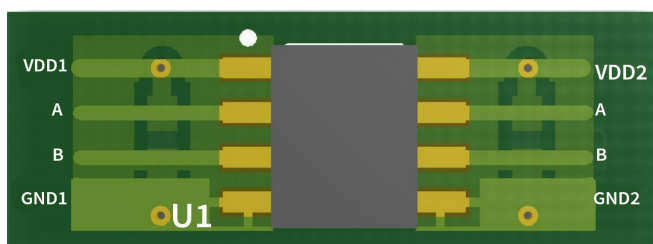


Figure8.2 Recommended PCB Layout — Top Layer



Figure8.3 Recommended PCB Layout — Bottom Layer

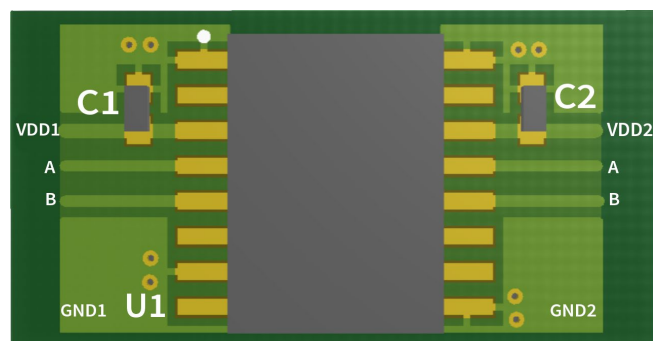


Figure8.4 Recommended PCB Layout — Top Layer

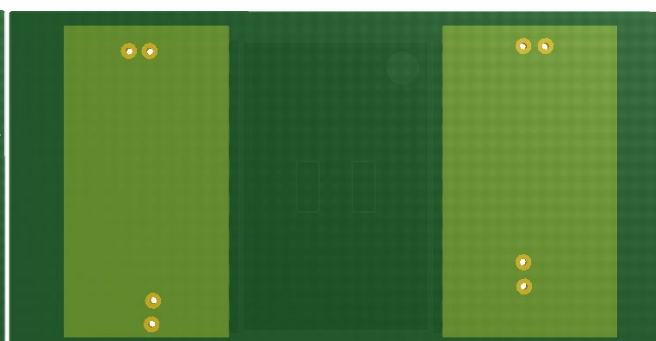


Figure8.5 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

Figure 8.6 shows the eye diagram of NSI822x at 50Mbps data rate output. The result shows a typical measurement on NSI822x with low jitter and wide open eye characteristics.

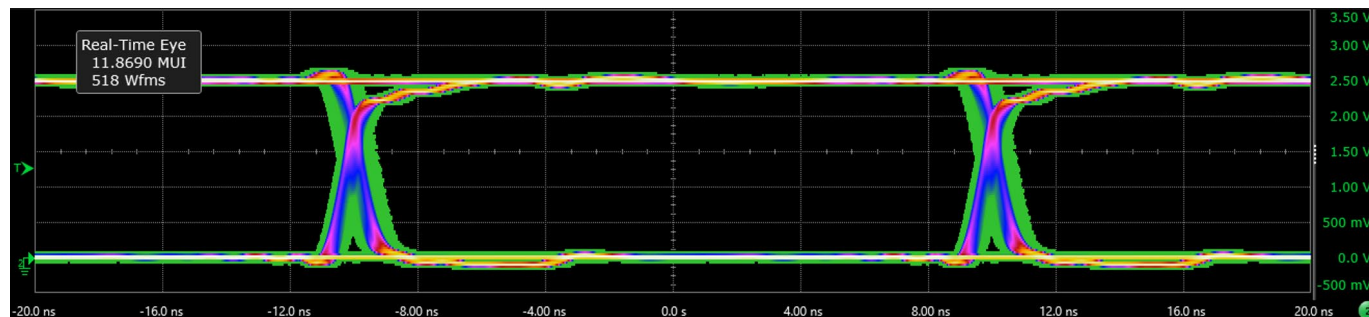


Figure 8.6 Eye Diagram at 50Mbps PRBS 2¹⁶-1, 2.5V and 25°C

8.4. Typical Supply Current Equations

The typical supply current of NSI822x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSI8220:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD2 * f * C_L * c1 * 10^{-9}$$

When $a1$ is the channel number of default state input at side 1, $b1$ is the channel number of non-default state input at side 1, $c1$ is the channel number of switch signal input at side 1.

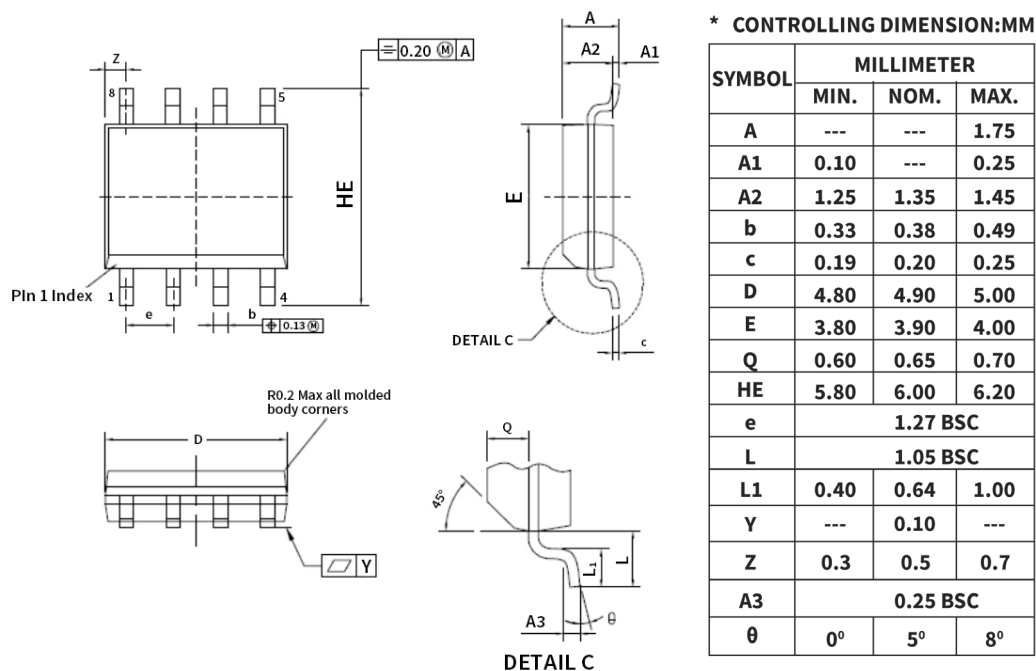
NSI8221/ NSI8222:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When $b1$ is the channel number of non-default state input at side 1, $c1$ is the channel number of switch signal input at side 1, $b2$ is the channel number of non-default state input at side 2, $c2$ is the channel number of switch signal input at side 2.

9. Package Information



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.1 SOP8 Package Shape and Dimension in millimeters

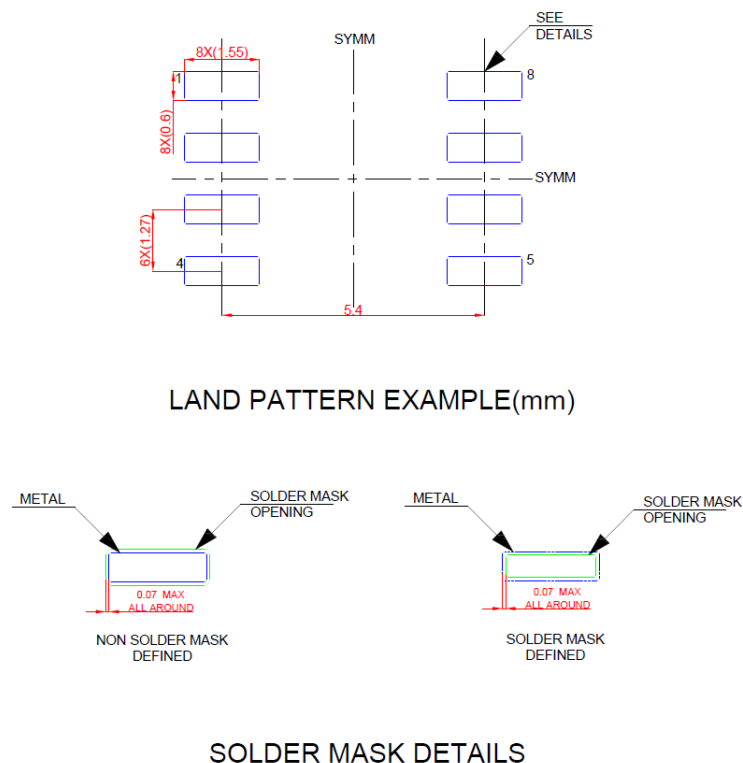
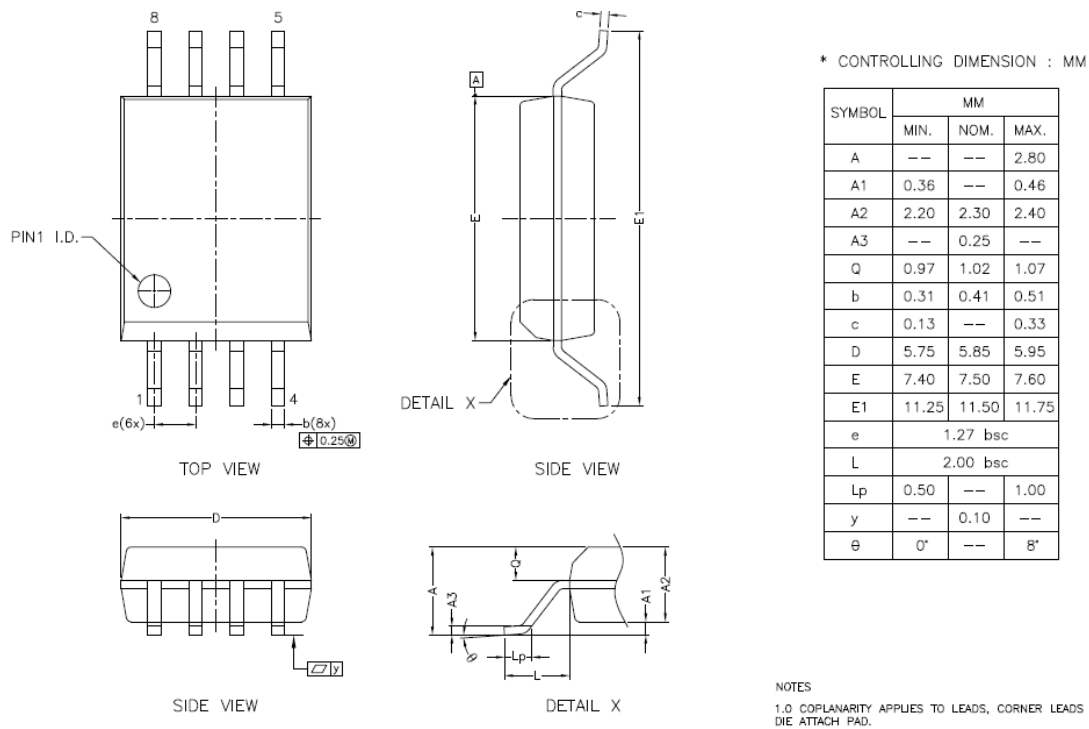


Figure 9.2 SOP8 Package Board Layout Example



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.3 SOW8 Package Shape and Dimension in millimeters

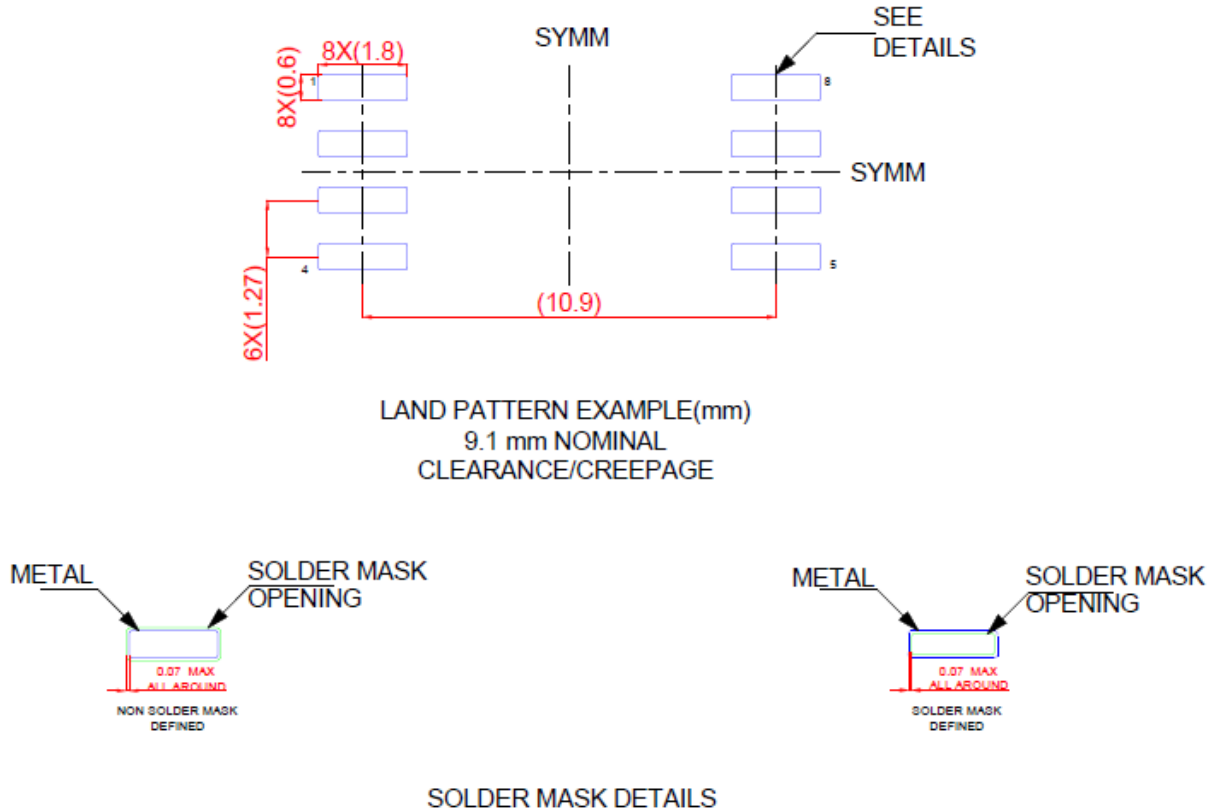
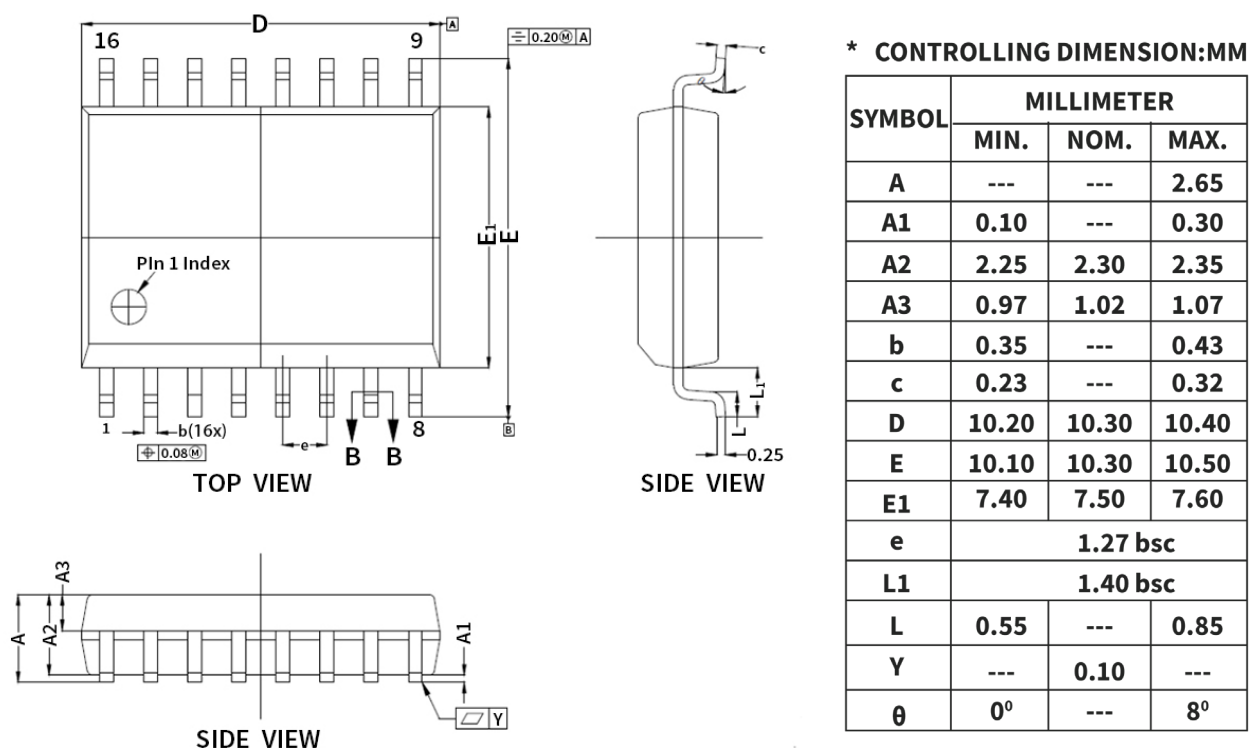


Figure 9.4 SOW8 Package Board Layout Example



NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.

Figure 9.5 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

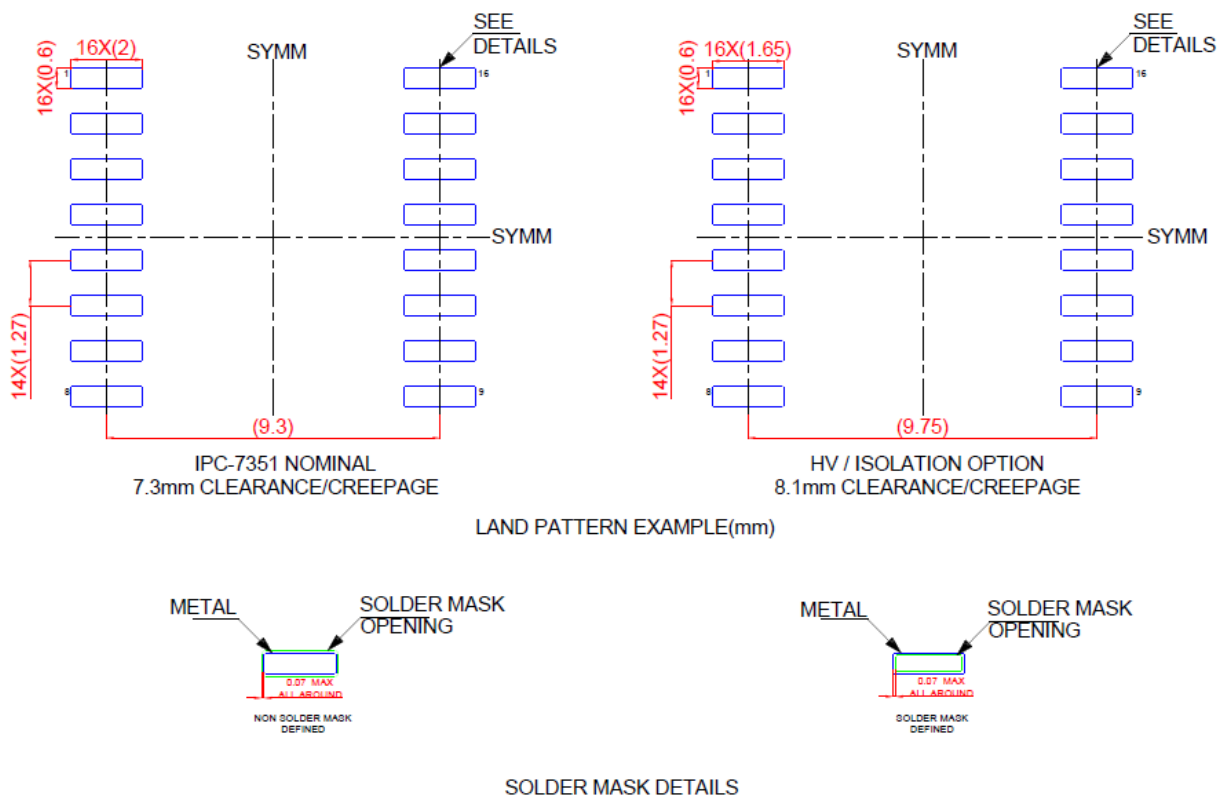
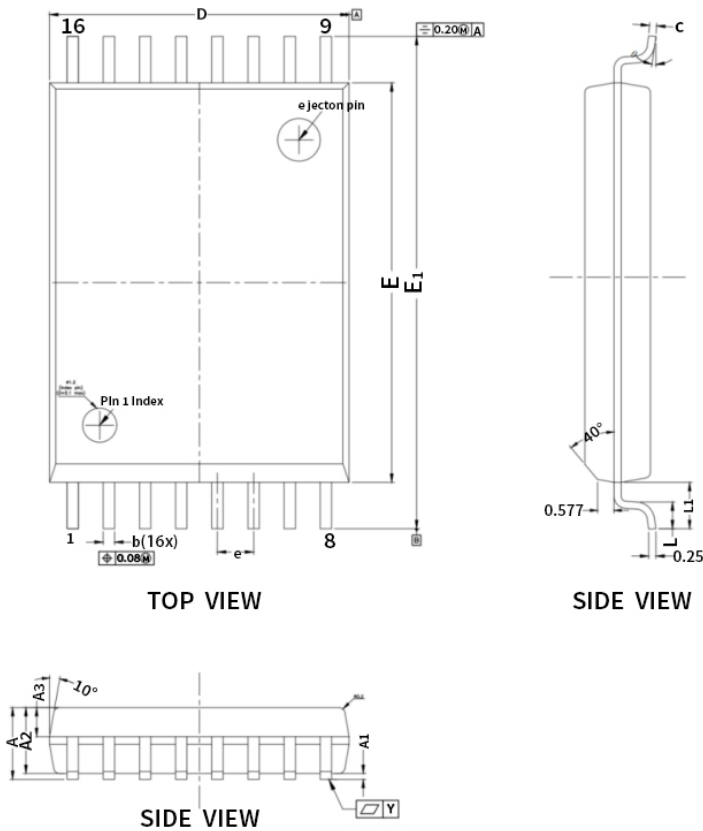


Figure 9.6 SOP16(300mil)/SOW16 Package Board Layout Example



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.42	10.52	10.62
E	13.9	14.0	14.1
E1	17.1	---	17.4
e	1.27 bsc		
L1	1.625 bsc		
L	0.6	---	1.1
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPWNARITY APPUES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

NOTE: This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side

Figure 9.7 SOP16(600mil)/SOWW16 Package Shape and Dimension in millimeters

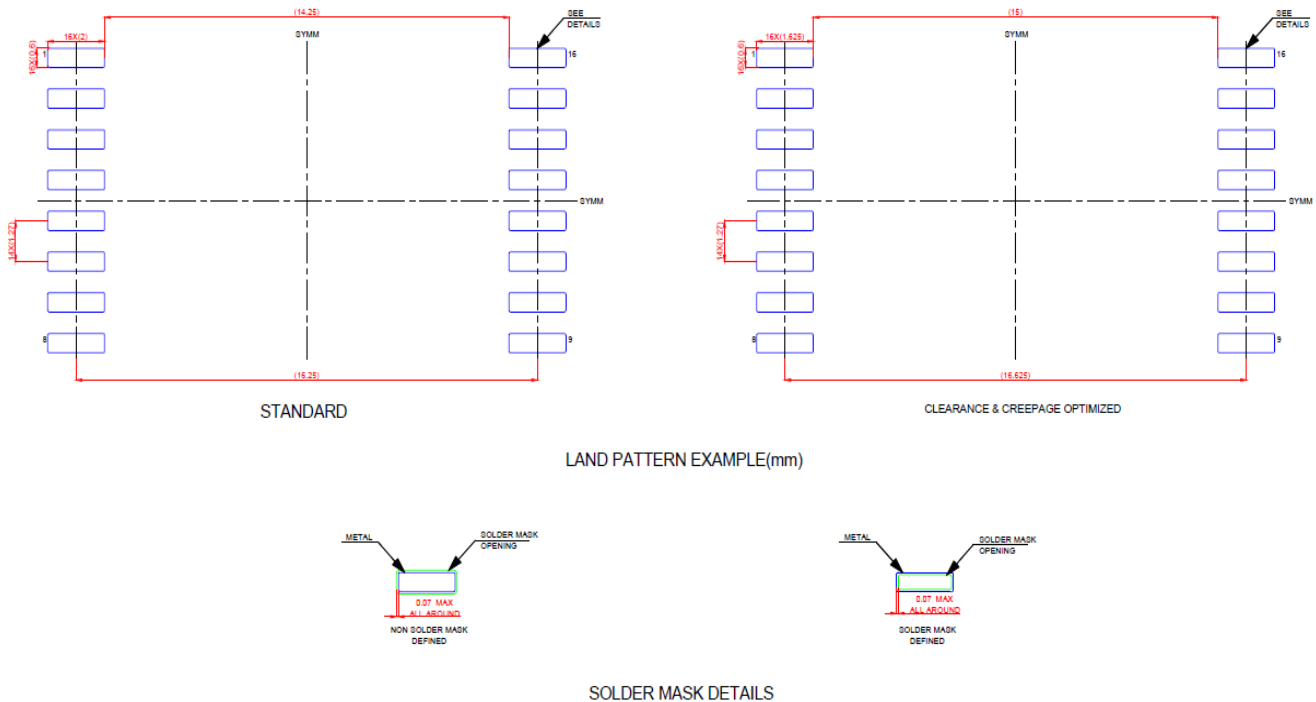


Figure 9.8 SOP16(600mil)/SOWW16 Package Board Layout Example

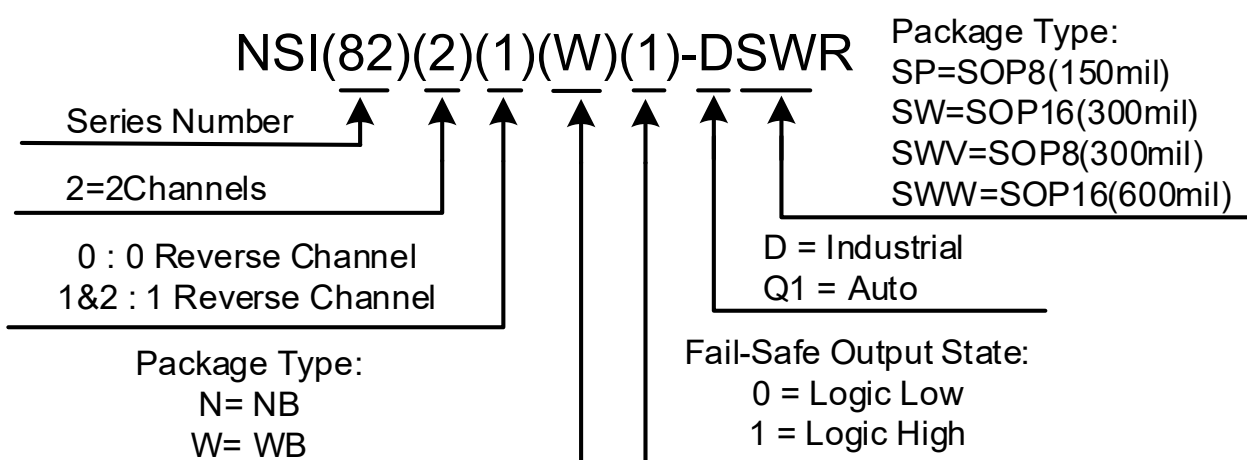
10. Order Information

<i>Part Number</i>	<i>Isolation Rating (kV)</i>	<i>Number of side 1 inputs</i>	<i>Number of side 2 inputs</i>	<i>Max Data Rate (Mbps)</i>	<i>Default Output State</i>	<i>Temperature</i>	<i>MSL</i>	<i>Package Type</i>	<i>Package Drawing</i>	<i>SPQ</i>
NSI8220N0-DSPR	3.75	2	0	150	Low	-55 to 125°C	1	SOP8 (150mil)	SOP8	2500
NSI8220N1-DSPR	3.75	2	0	150	High	-55 to 125°C	1	SOP8 (150mil)	SOP8	2500
NSI8221N0-DSPR	3.75	1	1	150	Low	-55 to 125°C	1	SOP8 (150mil)	SOP8	2500
NSI8221N1-DSPR	3.75	1	1	150	High	-55 to 125°C	1	SOP8 (150mil)	SOP8	2500
NSI8222N0-DSPR	3.75	1	1	150	Low	-55 to 125°C	1	SOP8 (150mil)	SOP8	2500
NSI8222N1-DSPR	3.75	1	1	150	High	-55 to 125°C	1	SOP8 (150mil)	SOP8	2500
NSI8220W0-DSWR	5	2	0	150	Low	-55 to 125°C	2	SOW16 (300mil)	SOW16	1000
NSI8220W1-DSWR	5	2	0	150	High	-55 to 125°C	2	SOW16 (300mil)	SOW16	1000
NSI8221W0-DSWR	5	1	1	150	Low	-55 to 125°C	2	SOW16 (300mil)	SOW16	1000
NSI8221W1-DSWR	5	1	1	150	High	-55 to 125°C	2	SOW16 (300mil)	SOW16	1000
NSI8222W0-DSWR	5	1	1	150	Low	-55 to 125°C	2	SOW16 (300mil)	SOW16	1000
NSI8222W1-DSWR	5	1	1	150	High	-55 to 125°C	2	SOW16 (300mil)	SOW16	1000
NSI8220W0-DSWVR	5	2	0	150	Low	-55 to 125°C	3	SOW8 (300mil)	SOW8	1000
NSI8220W1-DSWVR	5	2	0	150	High	-55 to 125°C	3	SOW8 (300mil)	SOW8	1000
NSI8221W0-DSWVR	5	1	1	150	Low	-55 to 125°C	3	SOW8 (300mil)	SOW8	1000
NSI8221W1-DSWVR	5	1	1	150	High	-55 to 125°C	3	SOW8 (300mil)	SOW8	1000
NSI8222W0-DSWVR	5	1	1	150	Low	-55 to 125°C	3	SOW8 (300mil)	SOW8	1000
NSI8222W1-DSWVR	5	1	1	150	High	-55 to 125°C	3	SOW8 (300mil)	SOW8	1000
NSI8220W0-DSWWR	8	2	0	150	Low	-55 to 125°C	3	SOW16 (600mil)	SOWW1 6	1000
NSI8220W1-DSWWR	8	2	0	150	High	-55 to 125°C	3	SOW16 (600mil)	SOWW1 6	1000
NSI8221W0-DSWWR	8	1	1	150	Low	-55 to 125°C	3	SOW16 (600mil)	SOWW1 6	1000
NSI8221W1-DSWWR	8	1	1	150	High	-55 to 125°C	3	SOW16 (600mil)	SOWW1 6	1000
NSI8222W0-DSWWR	8	1	1	150	Low	-55 to 125°C	3	SOW16 (600mil)	SOWW1 6	1000

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8222W1-DSWWR	8	1	1	150	High	-55 to 125°C	3	SOW16 (600mil)	SOWW1 6	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

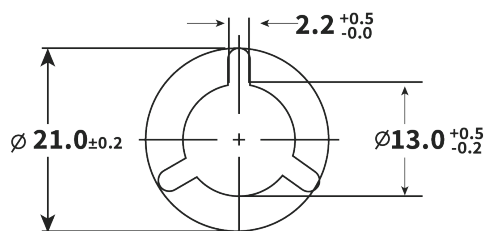
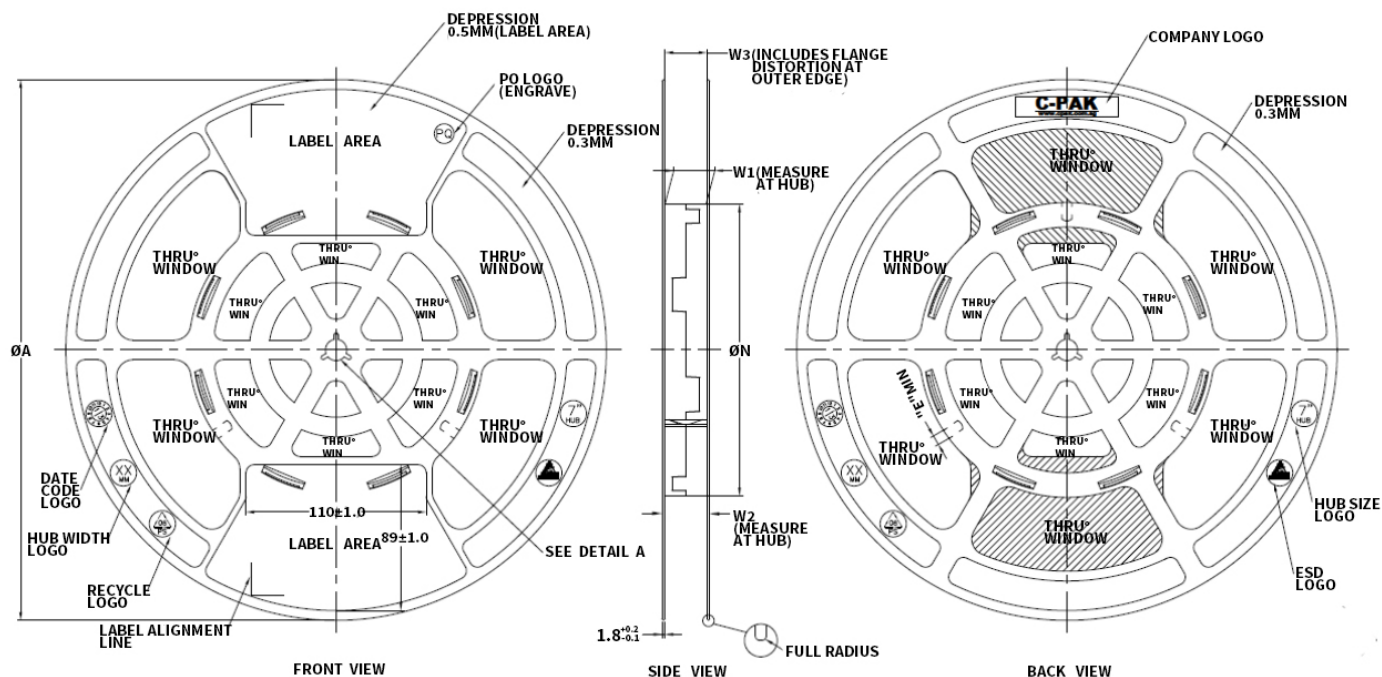
Part Number Rule:



11. Documentation Support

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSI822x	tbd	tbd	tbd	tbd

12. Tape and Reel Information

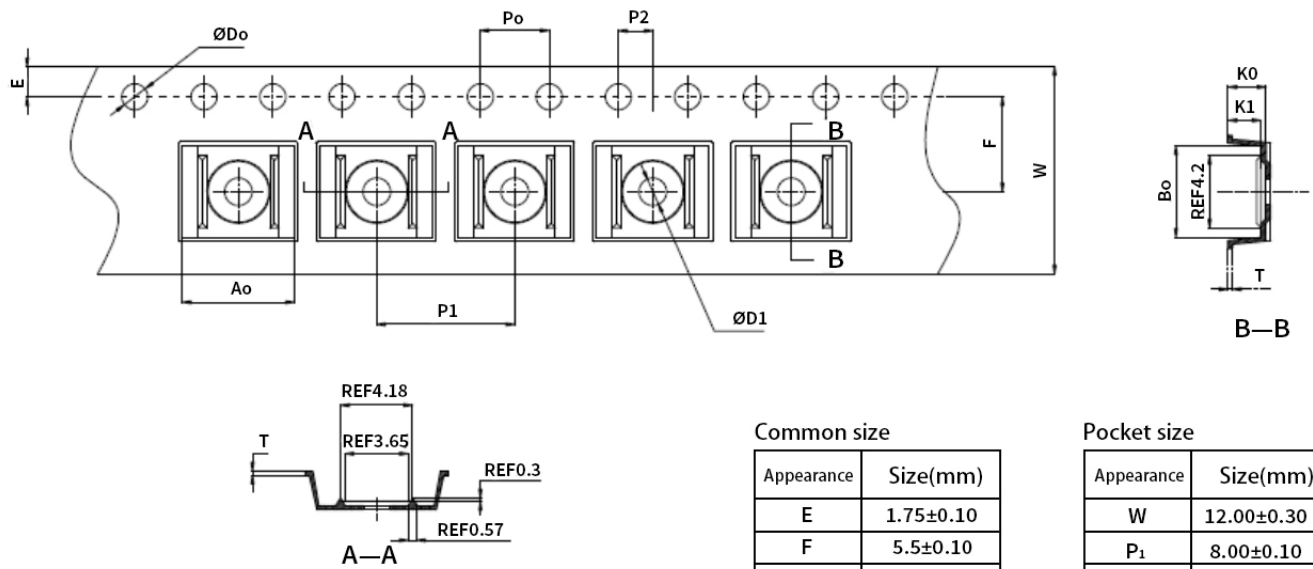


**ARBOR HOLE
DETAIL A
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	Ø A ±2.0	Ø N ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 ^{+1.5} _{-0.0}	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 ^{+2.0} _{-0.0}	18.4		5.5
16MM	330	178	16.4 ^{+2.0} _{-0.0}	22.4		5.5
24MM	330	178	24.4 ^{+2.0} _{-0.0}	30.4		5.5
32MM	330	178	32.4 ^{+2.0} _{-0.0}	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 ¹²	ANTISTATIC	ALL TYPES
B	10 ⁶ TO 10 ¹¹	STATIC DISSIPATIVE	BLACK ONLY
C	10 ⁵ & BELOW 10 ⁵	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10 ⁹ TO 10 ¹¹	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



Common size

Appearance	Size(mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Pocket size

Appearance	Size(mm)
W	12.00±0.30
P1	8.00±0.10
Ao	6.50±0.10
Bo	5.30±0.10
Ko	2.20±0.10
K1	1.90±0.10
T	0.30±0.05

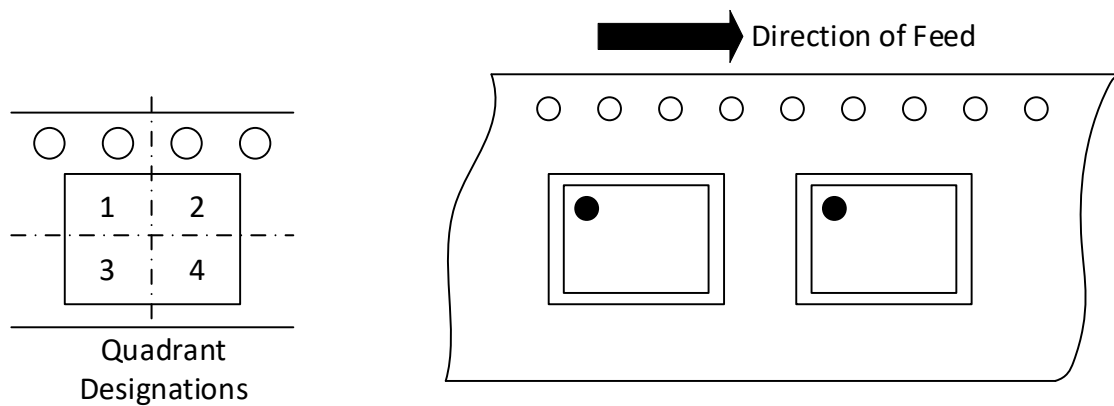
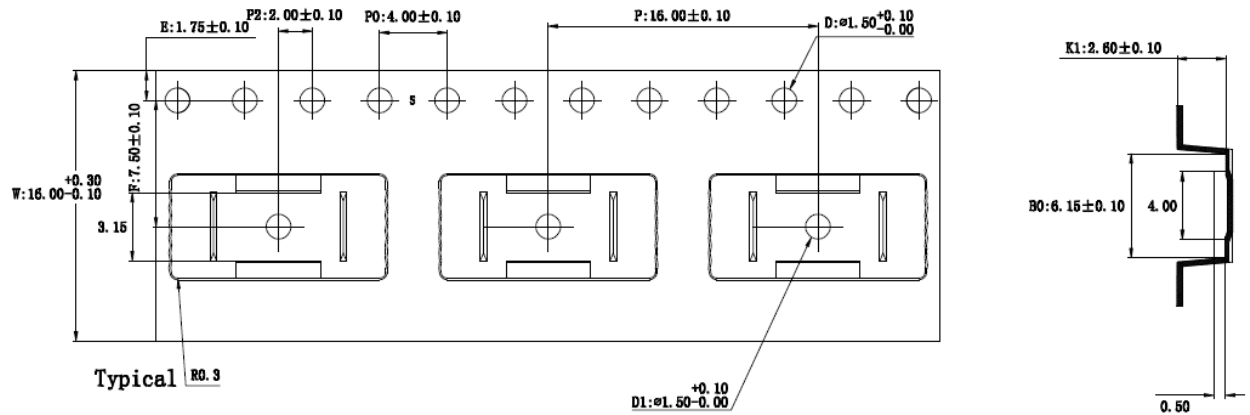


Figure 12.2 Tape Information of SOP8



技术要求:

Technical Requirements:

- 每10个料带链孔直径累计公差为 ± 0.20 毫米。
10 sprocket hole pitch cumulative toleran ± 0.20 mm
- 料带弯曲每250毫米不可超过1毫米。
Carrier camber is within 1 mm in 250 mm
- 所有尺寸符合EIA-481-D标准要求。
All dimensions meet EIA-481-D requirements

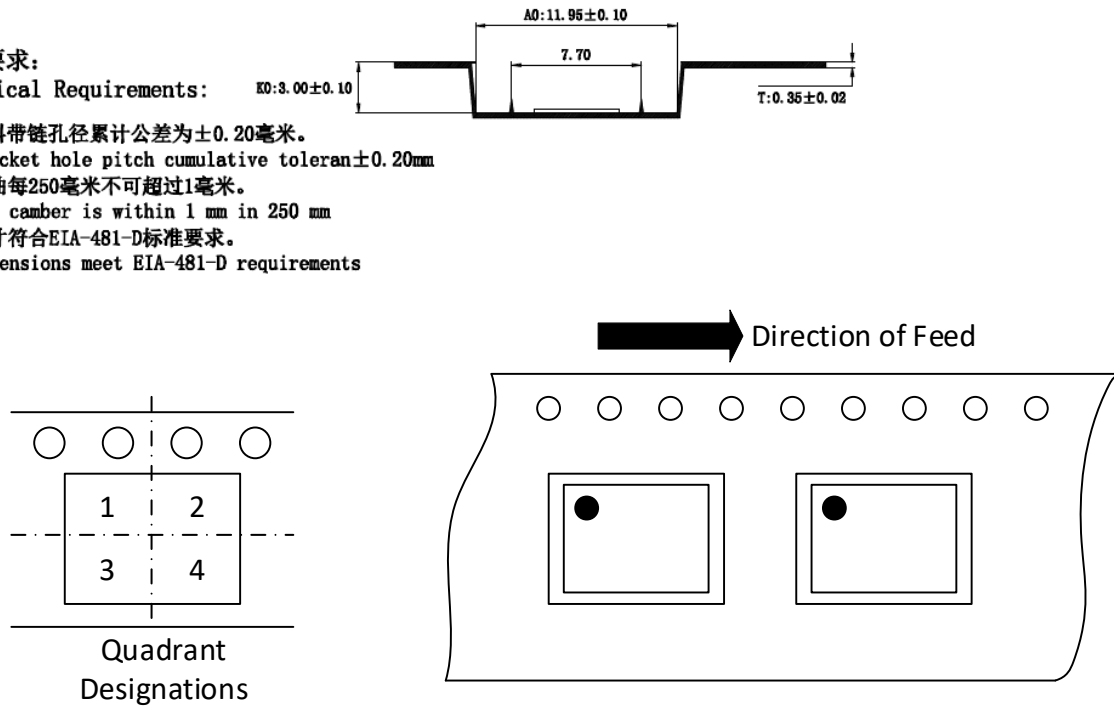
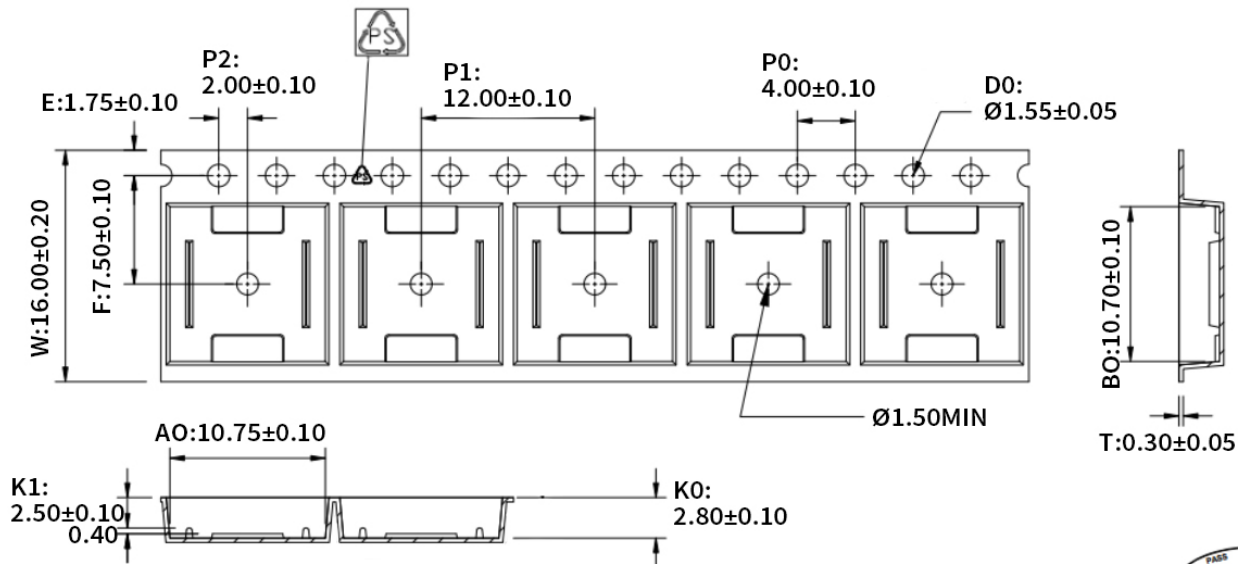


Figure 12.3 Tape Information of SOW8



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Packing length per 22" reel: 378 Meters. (Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity: $10^5 \sim 10^{10} \Omega/\square$



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

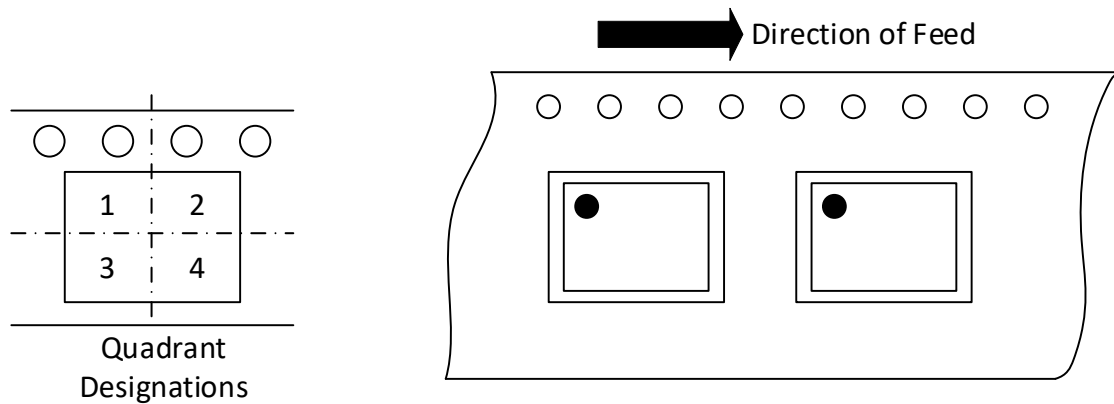
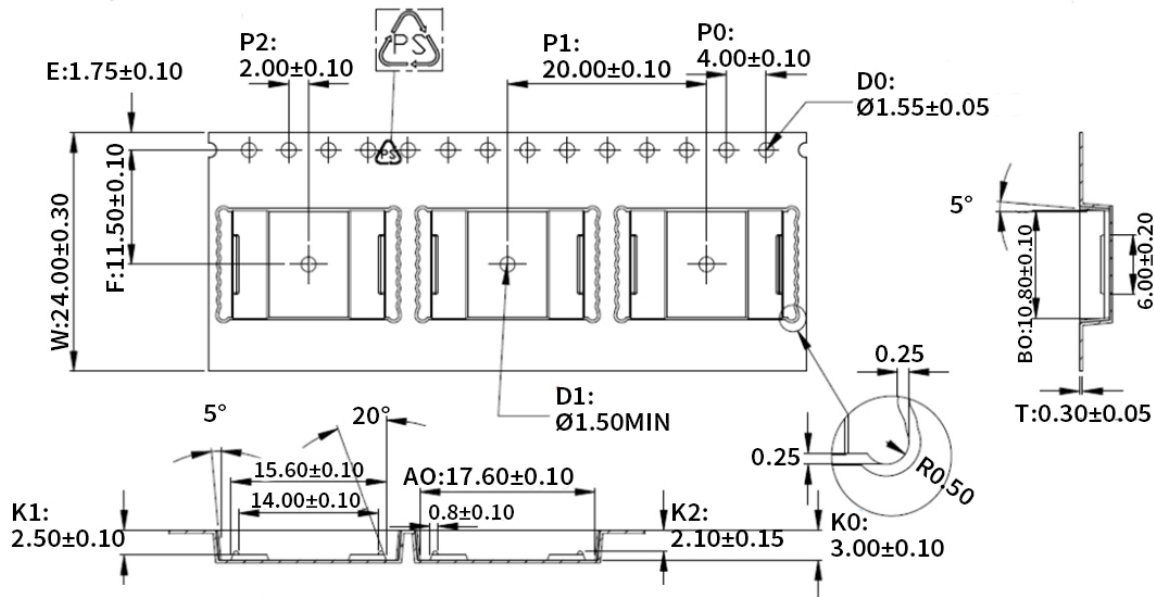


Figure 12.4 Tape Information of SOW16



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Packing length per 19" reel: 246.0 Meters. (Rewind 1:13)
7. Component load per 13" reel: 5000 pcs.
8. Surface resistivity: $10^5 \sim 10^{10} \Omega/\square$

W	24.00±0.30
A0	17.60±0.10
B0	10.80±0.10
K0	3.00±0.10
K1	2.50±0.10

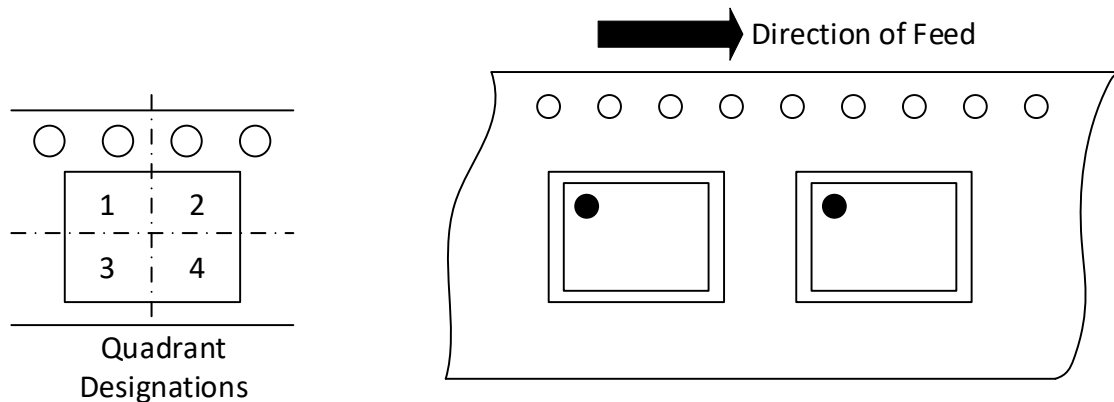


Figure 12.5 Tape Information of SOWW16

13. Revision History

<i>Revision</i>	<i>Description</i>	<i>Date</i>
1.0	Initial version	2019/12/20
1.1	Update SOW8 package PIN description	2020/6/23
1.2	Changed tape and reel information	2021/2/4
1.3	Operating temperature support -55 to 125 °C	2021/7/7
1.4	Update SOWW16 package	2021/12/5
1.5	Update Package Board Layout Example. Changed AEC-Q100 description.	2022/4/16
1.6	Update SOWW16 MSL, Pin Configuration and VISO.	2022/9/30
1.7	Correct formatting and images. Update Safety certification info throughout the document. Update Package Information and Tape and Reel Information. Update Function Description.	2024/8/23
1.8	Correct formatting and images. Update Input characteristics. Update eye diagram.	2025/1/13

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