

Product Overview

The NSI826x devices are high reliability six-channel digital isolators. The NSI826x device is safety certified by UL1577 support several insulation withstand voltage(3kV,5kV), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI826x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSI826x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI826x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 200kV/us
- Chip level ESD: HBM: ±8kV
- High system level EMC performance:
Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -55°C~125°C
- RoHS-compliant packages:
SOP16(300mil)
SSOP16

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN EN IEC 60747-17 (VDE 0884-17)

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation

Device Information

Part Number	Package	Body Size
NSI826xWx-DSWR	SOP16(300mil)	10.30mm × 7.50mm
NSI826xSx-DSSR	SSOP16	4.90mm × 3.90mm

Functional Block Diagrams

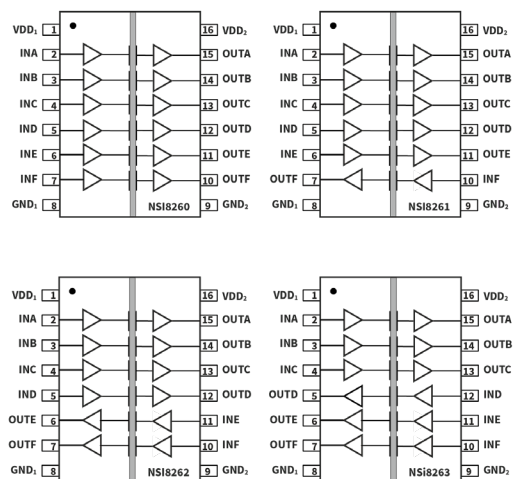


Figure 1. NSI826x Block Diagram

INDEX

1. PIN CONFIGURATION AND FUNCTIONS	3
2. ABSOLUTE MAXIMUM RATINGS	4
3. RECOMMENDED OPERATING CONDITIONS	5
4. THERMAL CHARACTERISTICS	5
5. SPECIFICATIONS	6
5.1. ELECTRICAL CHARACTERISTICS	6
5.2. SUPPLY CURRENT CHARACTERISTICS – 5V SUPPLY	6
5.3. SUPPLY CURRENT CHARACTERISTICS –3.3V SUPPLY.....	8
5.4. SUPPLY CURRENT CHARACTERISTICS–2.5V SUPPLY	10
5.5. SWITCHING CHARACTERISTICS - 5V SUPPLY.....	11
5.6. SWITCHING CHARACTERISTICS - 3.3V SUPPLY.....	12
5.7. SWITCHING CHARACTERISTICS - 2.5V SUPPLY.....	12
5.8. TYPICAL PERFORMANCE CHARACTERISTICS	13
5.9. PARAMETER MEASUREMENT INFORMATION.....	14
6. HIGH VOLTAGE FEATURE DESCRIPTION	15
6.1. INSULATION AND SAFETY RELATED SPECIFICATIONS.....	15
6.2. INSULATION CHARACTERISTICS	16
6.3. SAFETY-LIMITING VALUES.....	17
6.4. REGULATORY INFORMATION	19
7. FUNCTION DESCRIPTION	20
7.1. OVERVIEW	20
7.2. OOK MODULATION.....	21
8. APPLICATION NOTE	22
8.1. TYPICAL APPLICATION CIRCUIT	22
8.2. PCB LAYOUT	22
8.3. HIGH SPEED PERFORMANCE	23
8.4. TYPICAL SUPPLY CURRENT EQUATIONS.....	23
9. PACKAGE INFORMATION	24
10. ORDER INFORMATION	26
11. DOCUMENTATION SUPPORT	27
12. TAPE AND REEL INFORMATION	28
13. REVISION HISTORY	31

1. Pin Configuration and Functions

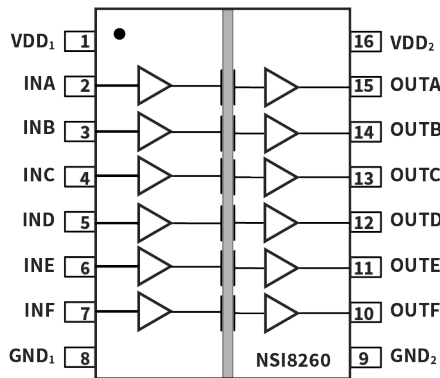


Figure 1.1 NSI8260 Package

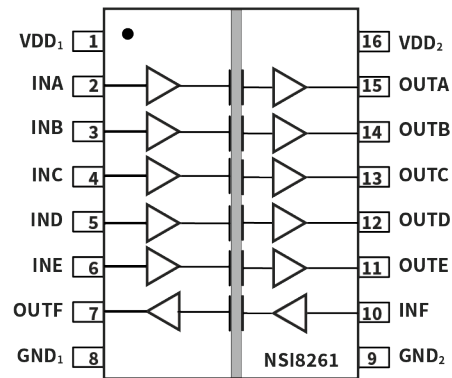


Figure 1.2 NSI8261 Package

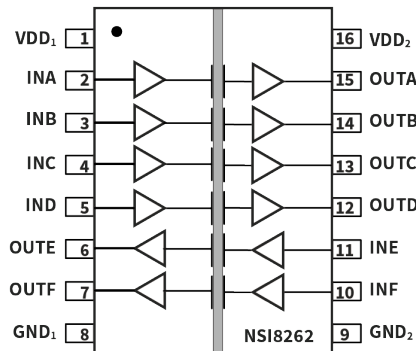


Figure 1.3 NSI8262 Package

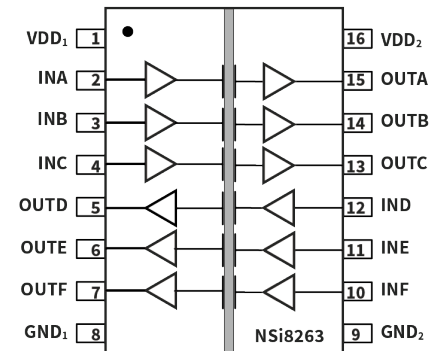


Figure 1.4 NSI8263 Package

Table 1.1 NSI8260/ NSI8261/ NSI8262 Pin Configuration and Description

NSI8260 PIN NO.	NSI8261 PIN NO.	NSI8262 PIN NO.	NSI8263 PIN NO.	SYMBOL	FUNCTION
1	1	1	1	VDD ₁	Power Supply for Isolator Side 1
2	2	2	2	INA	Logic Input A
3	3	3	3	INB	Logic Input B
4	4	4	4	INC	Logic Input C
5	5	5	12	IND	Logic Input D
6	6	11	11	INE	Logic Input E
7	10	10	10	INF	Logic Input F
8	8	8	8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	9	9	9	GND ₂	Ground 2, the ground reference for Isolator Side 2

NSI8260 PIN NO.	NSI8261 PIN NO.	NSI8262 PIN NO.	NSI8263 PIN NO.	SYMBOL	FUNCTION
10	7	7	7	OUTF	Logic Output F
11	11	6	6	OUTE	Logic Output E
12	12	12	5	OUTD	Logic Output D
13	13	13	13	OUTC	Logic Output C
14	14	14	14	OUTB	Logic Output B
15	15	15	15	OUTA	Logic Output A
16	16	16	16	VDD2	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND, VINE, VINF	-0.4		VDD+0.4	V	
Maximum Output Voltage	VOUTA, VOUTB, VOUTC, VOUTD, VOUTE, VOUTF	-0.4		VDD+0.4	V	
Maximum Input/Output Pulse Voltage	ALL I/O Pin	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Operating Temperature	T _{opr}	-55		125	°C	
Junction Temperature	T _j			150	°C	
Storage Temperature	T _{stg}	-65		150	°C	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

<i>Parameters</i>	<i>Symbol</i>	<i>min</i>	<i>typ</i>	<i>max</i>	<i>unit</i>
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	T _{opr}	-55		125	°C
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			150	Mbps

4. Thermal Characteristics

<i>Parameters</i>	<i>Symbol</i>	<i>SOP16(300mil)</i>	<i>SSOP16</i>	<i>Unit</i>
IC Junction-to-Air Thermal Resistance	θ_{JA}	60.3	86.5	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC (top)}$	24.0	26.9	°C/W
Junction-to-board thermal resistance	θ_{JB}	29.3	36.6	°C/W

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD _{POR}	2	2.2	2.4	V	POR threshold as during power-up
	VDD _{HYS}		0.1		V	POR threshold Hysteresis
Rising input switching threshold	V _{IT+}		1.6	2	V	
Falling input switching threshold	V _{IT-}	0.8	1.2		V	
Input threshold voltage hysteresis	V _{I(HYS)}		0.4		V	
High Level Output Voltage	V _{OH}	VDD-0.4			V	I _{OH} = - 4mA
Low Level Output Voltage	V _{OL}			0.4	V	I _{OL} = 4mA
Output Impedance	R _{out}		50		ohm	
Input Pull high or low Current	I _{pull}		8	15	µA	
Start Up Time after POR	t _{rs}		10		µs	
Common Mode Transient Immunity	CMTI	±200	±250		kV/µs	See Figure 5.12 , C _L = 15pF

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8260					
	I _{DD1} (Q0)		1.39	3.09	mA	All Input 0V for NSI8260x0 Or All Input at supply for NSI8260x1
	I _{DD2} (Q0)		3.41	5.63	mA	
	I _{DD1} (Q1)		7.37	12.16	mA	All Input at supply for NSI8260x0 Or All Input 0V for NSI8260x1
	I _{DD2} (Q1)		3.49	5.76	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD1} (1M)		4.39	7.24	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.67	6.06	mA	
	I _{DD1} (10M)		4.71	7.77	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.66	9.34	mA	
	I _{DD1} (100M)		7.47	14.94	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		23.8	55.22	mA	
NSI8261						
	I _{DD1} (Q0)		1.73	2.85	mA	All Input 0V for NSI8261x0 Or All Input at supply for NSI8261x1
	I _{DD2} (Q0)		3.07	5.07	mA	
	I _{DD1} (Q1)		6.72	11.09	mA	All Input at supply for NSI8261x0 Or All Input 0V for NSI8261x1
	I _{DD2} (Q1)		4.14	6.83	mA	
	I _{DD1} (1M)		4.27	7.05	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.79	6.25	mA	
	I _{DD1} (10M)		4.87	8.03	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.50	9.08	mA	
	I _{DD1} (100M)		10.19	20.38	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		21.08	47.21	mA	
NSI8262						
	I _{DD1} (Q0)		2.06	3.40	mA	All Input 0V for NSI8262x0 Or All Input at supply for NSI8262x1
	I _{DD2} (Q0)		2.74	4.52	mA	
	I _{DD1} (Q1)		6.08	10.03	mA	All Input at supply for NSI8262x0 Or All Input 0V for NSI8262x1
	I _{DD2} (Q1)		4.78	7.89	mA	
	I _{DD1} (1M)		4.15	6.85	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.91	6.45	mA	
	I _{DD1} (10M)		5.03	8.29	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.34	8.82	mA	
	I _{DD1} (100M)		12.91	25.83	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		18.36	39.2	mA	
NSI8263						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD1} (Q0)		2.40	3.96	mA	All Input 0V for NSI8263x0 Or All Input at supply for NSI8263x1
	I _{DD2} (Q0)		2.40	3.96	mA	
	I _{DD1} (Q1)		5.43	8.96	mA	All Input at supply for NSI8263x0 Or All Input 0V for NSI8263x1
	I _{DD2} (Q1)		5.43	8.96	mA	
	I _{DD1} (1M)		4.03	6.65	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		4.03	6.65	mA	
	I _{DD1} (10M)		5.19	8.56	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		5.19	8.56	mA	
	I _{DD1} (100M)		15.64	31.27	mA	All Input with 100Mbps, C _L = 15pF
I _{DD2} (100M)		15.64	31.27	mA		

5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8260					
	I _{DD1} (Q0)		1.33	3.00	mA	All Input 0V for NSI8260x0 Or All Input at supply for NSI8260x1
	I _{DD2} (Q0)		3.36	5.54	mA	
	I _{DD1} (Q1)		7.26	11.98	mA	All Input at supply for NSI8260x0 Or All Input 0V for NSI8260x1
	I _{DD2} (Q1)		3.43	5.66	mA	
	I _{DD1} (1M)		4.31	7.11	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.55	5.86	mA	
	I _{DD1} (10M)		4.50	7.43	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.87	8.04	mA	
	I _{DD1} (100M)		6.15	12.30	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		18.89	37.78	mA	
	NSI8261					
	I _{DD1} (Q0)		1.67	2.75	mA	All Input 0V for NSI8261x0 Or All Input at supply for NSI8261x1
	I _{DD2} (Q0)		3.02	4.99	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD1} (Q1)		6.62	10.93	mA	All Input at supply for NSI8261x0 Or All Input 0V for NSI8261x1
	I _{DD2} (Q1)		4.07	6.71	mA	
	I _{DD1} (1M)		4.18	6.90	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.68	6.07	mA	
	I _{DD1} (10M)		4.56	7.53	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.81	7.93	mA	
	I _{DD1} (100M)		8.27	16.55	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		16.77	33.53	mA	
NSI8262						
	I _{DD1} (Q0)		2.01	3.31	mA	All Input 0V for NSI8261x0 Or All Input at supply for NSI8261x1
	I _{DD2} (Q0)		2.68	4.43	mA	
	I _{DD1} (Q1)		5.98	9.87	mA	All Input at supply for NSI8261x0 Or All Input 0V for NSI8261x1
	I _{DD2} (Q1)		4.71	7.77	mA	
	I _{DD1} (1M)		4.06	6.69	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.80	6.28	mA	
	I _{DD1} (10M)		4.62	7.63	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.75	7.83	mA	
	I _{DD1} (100M)		10.40	20.79	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		14.64	29.29	mA	
NSI8263						
	I _{DD1} (Q0)		2.35	3.87	mA	All Input 0V for NSI8262x0 Or All Input at supply for NSI8262x1
	I _{DD2} (Q0)		2.35	3.87	mA	
	I _{DD1} (Q1)		5.35	8.82	mA	All Input at supply for NSI8262x0 Or All Input 0V for NSI8262x1
	I _{DD2} (Q1)		5.35	8.82	mA	
	I _{DD1} (1M)		3.93	6.48	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.93	6.48	mA	
	I _{DD1} (10M)		4.69	7.73	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.69	7.73	mA	
	I _{DD1} (100M)		12.52	25.04	mA	All Input with 100Mbps,

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD2} (100M)		12.52	25.04	mA	C _L = 15pF

5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NSI8260					
	I _{DD1} (Q0)		1.29	2.94	mA	All Input 0V for NSI8260x0 Or All Input at supply for NSI8260x1
	I _{DD2} (Q0)		3.33	5.49	mA	
	I _{DD1} (Q1)		7.00	11.55	mA	All Input at supply for NSI8260x0 Or All Input 0V for NSI8260x1
	I _{DD2} (Q1)		3.39	5.59	mA	
	I _{DD1} (1M)		4.17	6.88	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.47	5.73	mA	
	I _{DD1} (10M)		4.29	7.08	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.48	7.39	mA	
	I _{DD1} (100M)		5.27	10.54	mA	All Input with 100Mbps, C _L =15pF
	I _{DD2} (100M)		15.33	30.66	mA	
	NSI8261					
	I _{DD1} (Q0)		1.63	2.69	mA	All Input 0V for NSI8261x0 Or All Input at supply for NSI8261x1
	I _{DD2} (Q0)		2.99	4.93	mA	
	I _{DD1} (Q1)		6.40	10.56	mA	All Input at supply for NSI8261x0 Or All Input 0V for NSI8261x1
	I _{DD2} (Q1)		3.99	6.59	mA	
	I _{DD1} (1M)		4.05	6.69	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.59	5.92	mA	
	I _{DD1} (10M)		4.32	7.13	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.45	7.34	mA	
	I _{DD1} (100M)		6.95	13.89	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		13.65	27.31	mA	
	NSI8262					

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	I _{DD1} (Q0)		1.97	3.25	mA	All Input 0V for NSI8261x0 Or All Input at supply for NSI8261x1
	I _{DD2} (Q0)		2.65	4.37	mA	
	I _{DD1} (Q1)		5.80	9.56	mA	All Input at supply for NSI8261x0 Or All Input 0V for NSI8261x1
	I _{DD2} (Q1)		4.59	7.58	mA	
	I _{DD1} (1M)		3.94	6.50	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.70	6.11	mA	
	I _{DD1} (10M)		4.35	7.18	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.42	7.29	mA	
	I _{DD1} (100M)		8.62	17.25	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		11.98	23.95	mA	
NSI8263						
	I _{DD1} (Q0)		2.31	3.81	mA	All Input 0V for NSI8262x0 Or All Input at supply for NSI8262x1
	I _{DD2} (Q0)		2.31	3.81	mA	
	I _{DD1} (Q1)		5.20	8.57	mA	All Input at supply for NSI8262x0 Or All Input 0V for NSI8262x1
	I _{DD2} (Q1)		5.20	8.57	mA	
	I _{DD1} (1M)		3.82	6.30	mA	All Input with 1Mbps, C _L =15pF
	I _{DD2} (1M)		3.82	6.30	mA	
	I _{DD1} (10M)		4.39	7.24	mA	All Input with 10Mbps, C _L =15pF
	I _{DD2} (10M)		4.39	7.24	mA	
	I _{DD1} (100M)		10.30	20.60	mA	All Input with 100Mbps, C _L = 15pF
	I _{DD2} (100M)		10.30	20.60	mA	

5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t _{PLH}	2.5	6.54	15	ns	See Figure 5.11 , C _L = 15pF

Parameters	Symbol	Min	Typ	Max	Unit	Comments
	t_{PHL}	2.5	8.30	15	ns	See Figure 5.11 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

5.6. Switching Characteristics - 3.3V Supply

($VDD1=3.3V \pm 10\%$, $VDD2=3.3V \pm 10\%$, $T_a=-55^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at **VDD1 = 3.3V**, **VDD2 = 3.3V**, $T_a = 25^\circ C$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	7.5	15	ns	See Figure 5.11 , $C_L = 15pF$
	t_{PHL}	2.5	8.7	15	ns	See Figure 5.11 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

5.7. Switching Characteristics - 2.5V Supply

($VDD1=2.5V \pm 10\%$, $VDD2=2.5V \pm 10\%$, $T_a=-55^\circ C$ to $125^\circ C$. Unless otherwise noted, Typical values are at **VDD1 = 2.5V**, **VDD2 = 2.5V**, $T_a = 25^\circ C$)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.11 , $C_L = 15pF$
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.11 , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Rising Time	t_r			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Falling Time	t_f			5.0	ns	See Figure 5.11 , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	

5.8. Typical Performance Characteristics

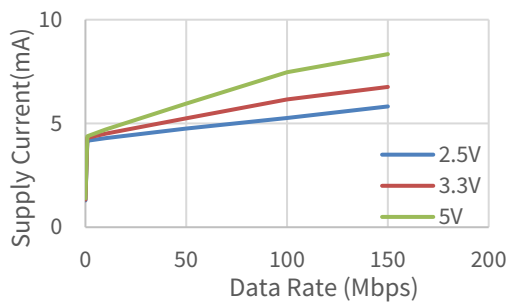


Figure 5.1 NSI8260 VDD1 Supply Current vs Data Rate

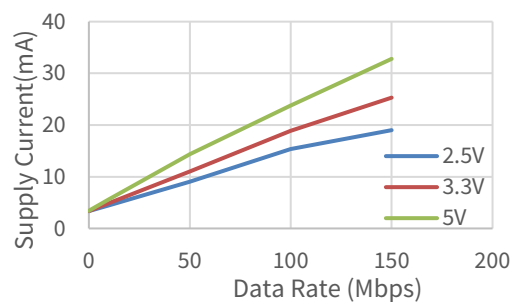


Figure 5.2 NSI8260 VDD2 Supply Current vs Data Rate

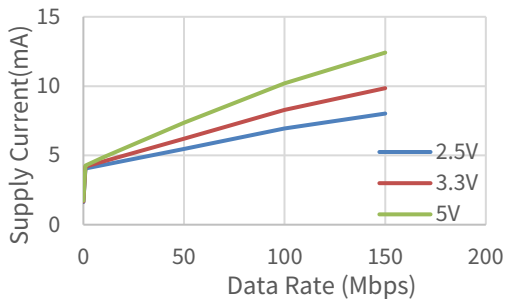


Figure 5.3 NSI8261 VDD1 Supply Current vs Data Rate

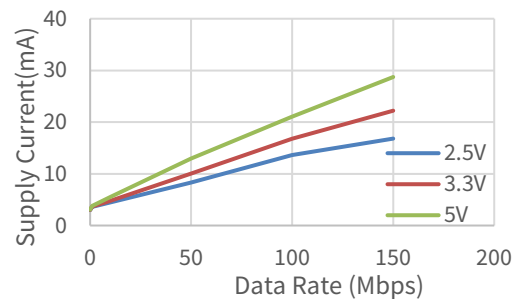


Figure 5.4 NSI8261 VDD2 Supply Current vs Data Rate

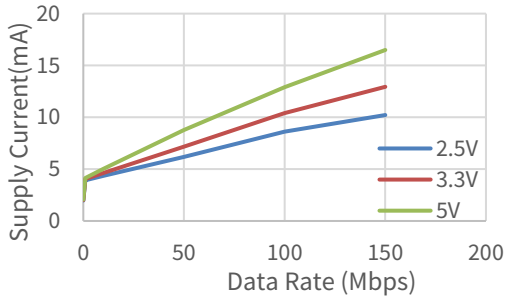


Figure 5.5 NSI8262 VDD1 Supply Current vs Data Rate

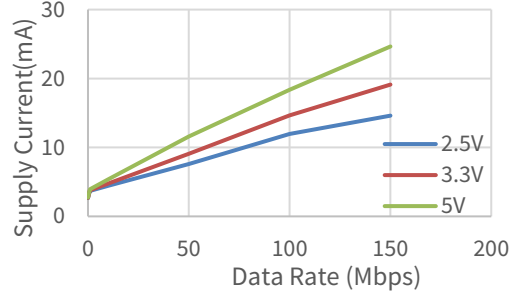


Figure 5.6 NSI8262 VDD2 Supply Current vs Data Rate

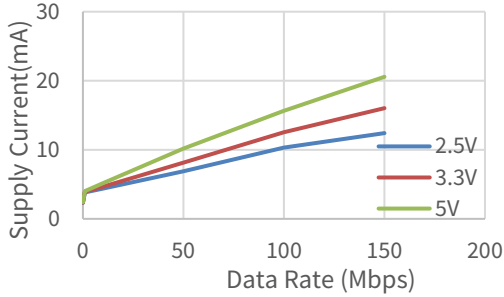


Figure 5.7 NSI8263 VDD1 Supply Current vs Data Rate

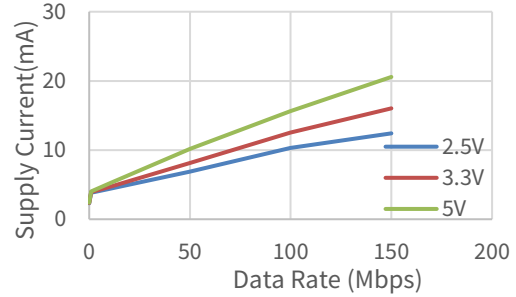


Figure 5.8 NSI8263 VDD2 Supply Current vs Data Rate

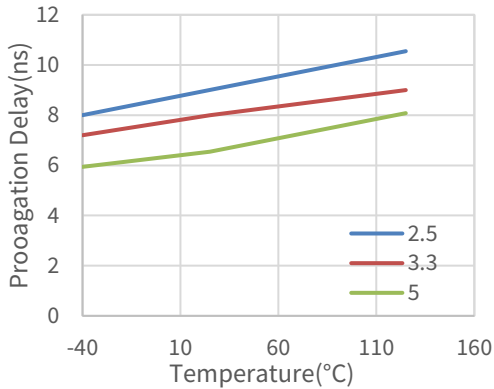


Figure 5.9 Rising Edge Propagation Delay Vs Temp

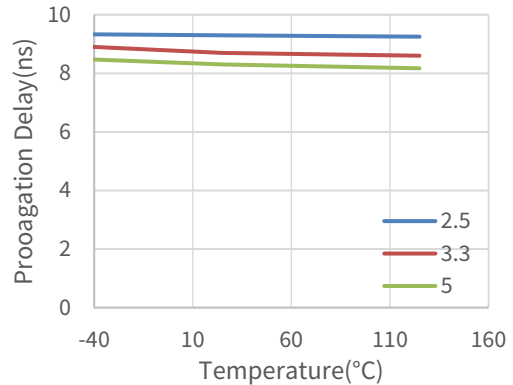
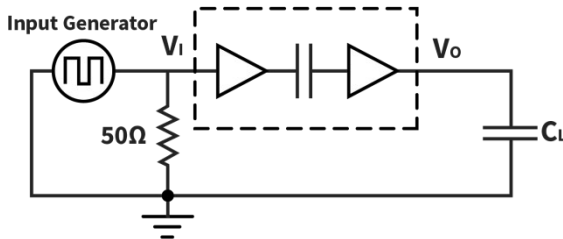


Figure 5.10 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information



(1) Input Generator Characteristics : PRR ≤ 50kHz, tr ≤ 3ns, tf ≤ 3ns, Duty cycle = 50%, Zo = 50 Ω.

Figure 5.11 Switching Characteristics Test Circuit and Waveform

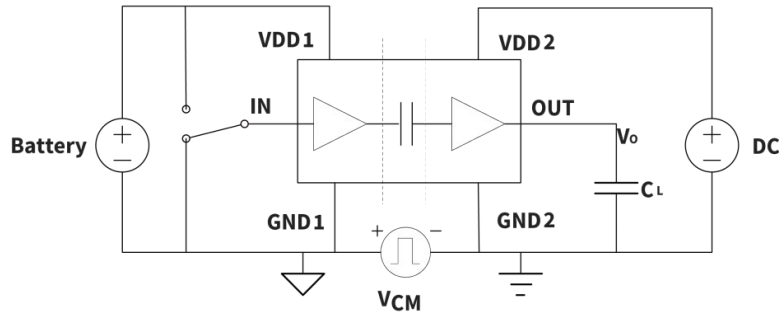


Figure 5.12 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	Symbol	Value		Unit	Comments
		SOP16 (300mil)	SSOP16		
Minimum External Clearance	CLR	8	3.9	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	8	3.9	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	28		µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			IEC 60664-1

Description	Test Condition	Value	
		SOP16 (300mil)	SSOP16
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV	I to III
	For Rated Mains Voltage ≤ 300Vrms	I to IV	I to II
	For Rated Mains Voltage ≤ 600Vrms	I to IV	I
	For Rated Mains Voltage ≤ 1000Vrms	I to III	/
Climatic Classification		40/125/21	
Pollution Degree per DIN VDE 0110		2	

6.2. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOP16 (300mil)	SSOP16	
Maximum repetitive isolation voltage		V_{IORM}	2121	565	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	400	V_{RMS}
	DC Voltage		2121	565	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{ s}$.	q_{pd}	<5	\	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10\text{ s}$				pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1\text{ s}$ $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1\text{ s}$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)				pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60\text{ s}$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10\text{ s}$.	q_{pd}	\	<5	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60\text{ s}$, $V_{pd(m)}=1.3*V_{IORM}$, $t_m=10\text{ s}$				pC
	Method b, routine test (100% production) and preconditioning (type				pC

Description	Test Condition	Symbol	Value		Unit
			SOP16 (300mil)	SSOP16	
	test); $V_{ini}=1.2 \cdot V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.5 \cdot V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)				
Maximum transient isolation voltage	$t = 60 \text{ sec}$	V_{IOTM}	8000	5000	V_{PEAK}
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	5384	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	7000	V_{PEAK}
Isolation resistance	$V_{IO} = 500V$, $T_{amb}=25^\circ C$	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	$V_{IO} = 500V$, $100^\circ C \leq T_{amb} \leq 125^\circ C$	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	$V_{IO} = 500V$, $T_{amb}=T_s$	R_{IO}	$>10^9$	$>10^9$	Ω
Isolation capacitance	$f = 1MHz$	C_{IO}	1.2	1.2	pF
UL1577					
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, $t = 60 \text{ s}$ (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1 \text{ s}$ (100% production test)	V_{ISO}	5000	3000	V_{RMS}

6.3. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI826x-DSWR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 60.3 \text{ }^\circ C/W$, $T_J = 150 \text{ }^\circ C$, $T_A = 25 \text{ }^\circ C$	2073	mW
Safety Supply Current	$R_{\theta JA} = 60.3 \text{ }^\circ C/W$, $V_I = 5V$, $T_J = 150 \text{ }^\circ C$, $T_A = 25 \text{ }^\circ C$	414	mA
Safety Temperature ²⁾		150	$^\circ C$

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

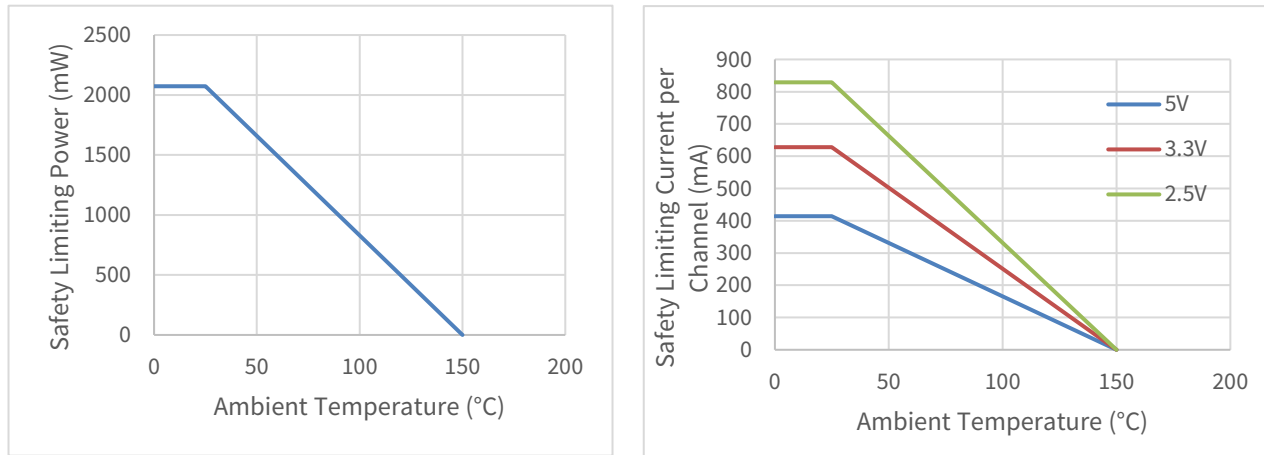


Figure 6.1 NSI826x-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSI826x-DSSR

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA} = 86.5 \text{ }^\circ\text{C/W}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$	1445	mW
Safety Supply Current	$R_{\theta JA} = 86.5 \text{ }^\circ\text{C/W}$, $V_I = 5\text{V}$, $T_J = 150 \text{ }^\circ\text{C}$, $T_A = 25 \text{ }^\circ\text{C}$	289	mA
Safety Temperature ²⁾		150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SSOP16 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

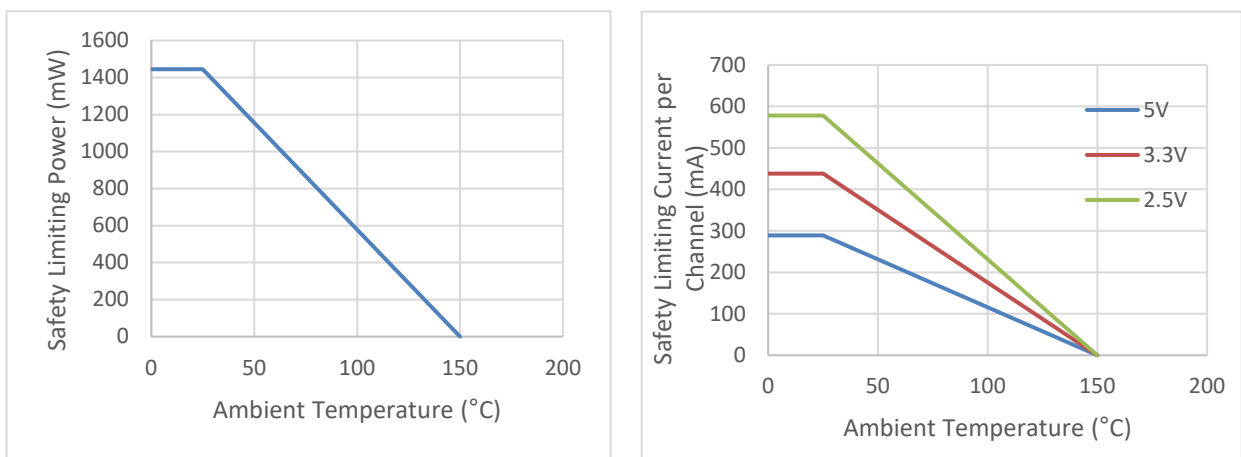


Figure 6.2 NSI826x-DSSR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.4. Regulatory Information

The NSI826xW-DSWR are approved or pending approval by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>	<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022	Certified According to EN IEC 62368-1
Single Protection, 5000V _{rms} Isolation voltage	Single Protection, 5000V _{rms} Isolation voltage	Reinforced Insulation V _{IORM} =2121V _{peak} V _{IOTM} =8000V _{peak} V _{IOSM} =10000V _{peak}	Reinforced insulation	5000V _{rms} for 1min
E500602	E500602	File (40052820)	CQC20001264939	R50574061

The NSI826xS-DSSR are approved or pending approval by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>	<i>TUV</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022	Certified According to EN IEC 62368-1
Single Protection, 3000V _{rms} Isolation voltage	Single Protection, 3000V _{rms} Isolation voltage	Basic Insulation V _{IORM} =565V _{peak} V _{IOTM} =5000V _{peak} V _{IOSM} =7000V _{peak}	Basic insulation	5000V _{rms} for 1min
E500602	E500602	File (40050121)	CQC19001233128	R50574061

7. Function Description

7.1. Overview

The NSI826x is a Six-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI826x devices are high reliability six-channel digital isolator. The NSI826x device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI826x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSI826x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI826x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI826x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 7.1 Output status vs. power status

<i>Input¹</i>	<i>VDDIN status</i>	<i>VDDOUT status</i>	<i>Output</i>	<i>Comment</i>
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI826xx0) H(NSI826xx1)	The output follows the same status with the input after input side VDD is powered on.
X	Ready	Unready	Undetermined	The output follows the same status with the input after output side VDD2 is powered on.
Note: H=Logic high; L=Logic low; X=Logic low or logic high VDDIN is input side power; VDDOUT is output side power. (1) There is a protection diode between the input and the VDDIN. When the VDDIN is floating, the strong drive signal through the input pin will put the VDDIN in an indeterminate state.				

7.2. OOK Modulation

NSI8266 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1 to Figure 7.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

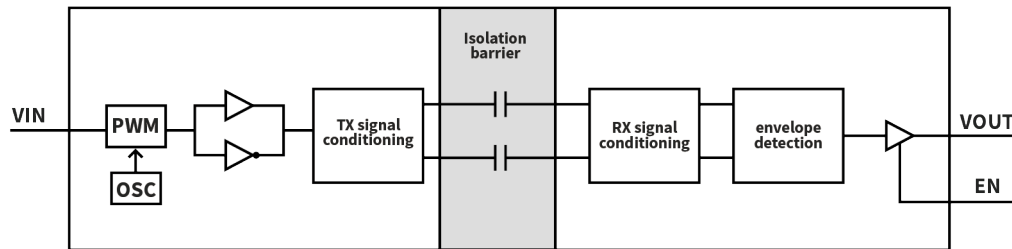


Figure 7.1 Single Channel Function Block Diagram

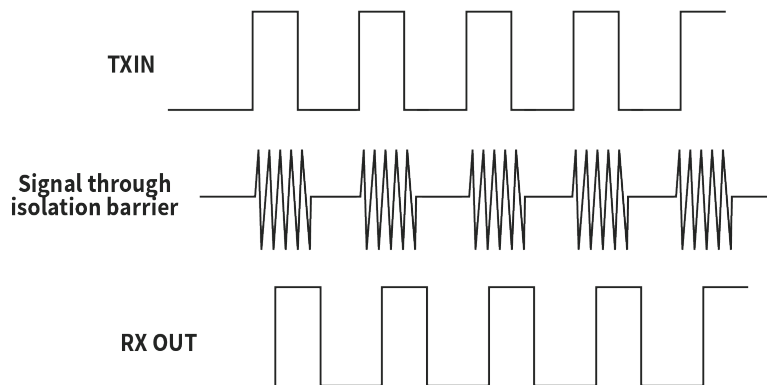


Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

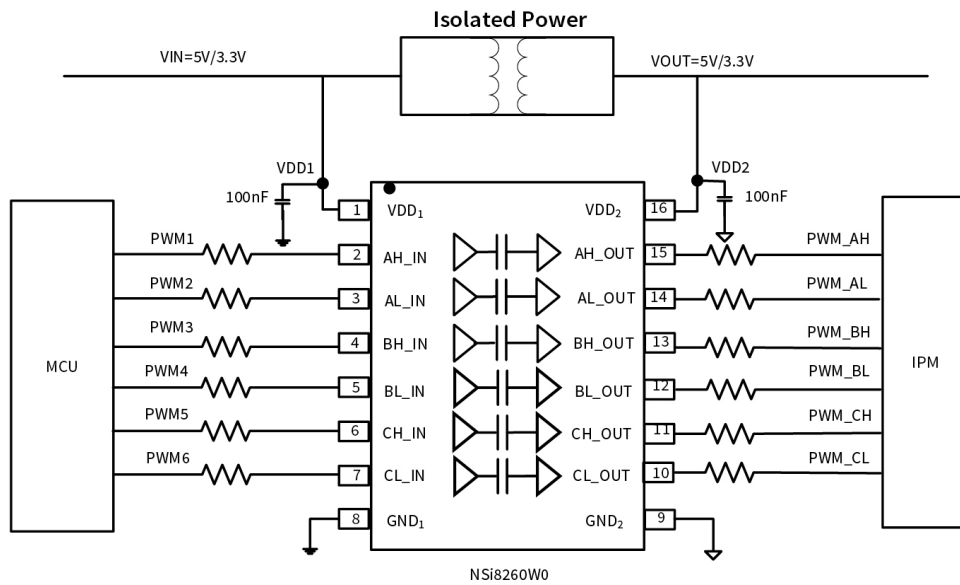


Figure 8.1 Typical PWM isolation circuit for IPM

8.2. PCB Layout

The NSI826x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

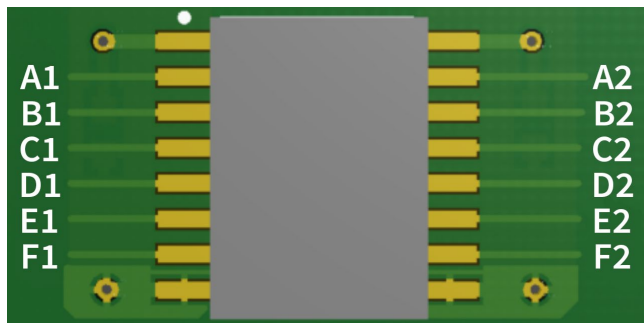


Figure 8.2 Recommended PCB Layout — Top Layer



Figure 8.3 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

Figure 8.4 shows the eye diagram of NSI826x at 50Mbps data rate output. The result shows a typical measurement on NSI826x with low jitter and wide open eye characteristics.

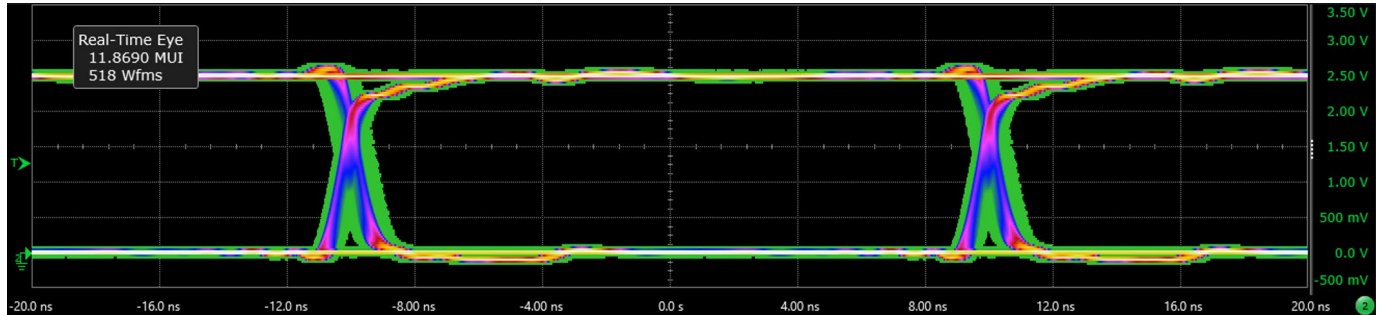


Figure 8.4 Eye Diagram at 50Mbps PRBS 2¹⁶-1, 2.5V and 25°C

8.4. Typical Supply Current Equations

The typical supply current of NSI826x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

NSI8260:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD2 * f * C_L * c1 * 10^{-9}$$

When a1 is the channel number of default state input at side 1, b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1.

NSI8261:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

NSI8262:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

NSI8263:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When b1 is the channel number of non-default state input at side 1, c1 is the channel number of switch signal input at side 1, b2 is the channel number of non-default state input at side 2, c2 is the channel number of switch signal input at side 2.

9. Package Information

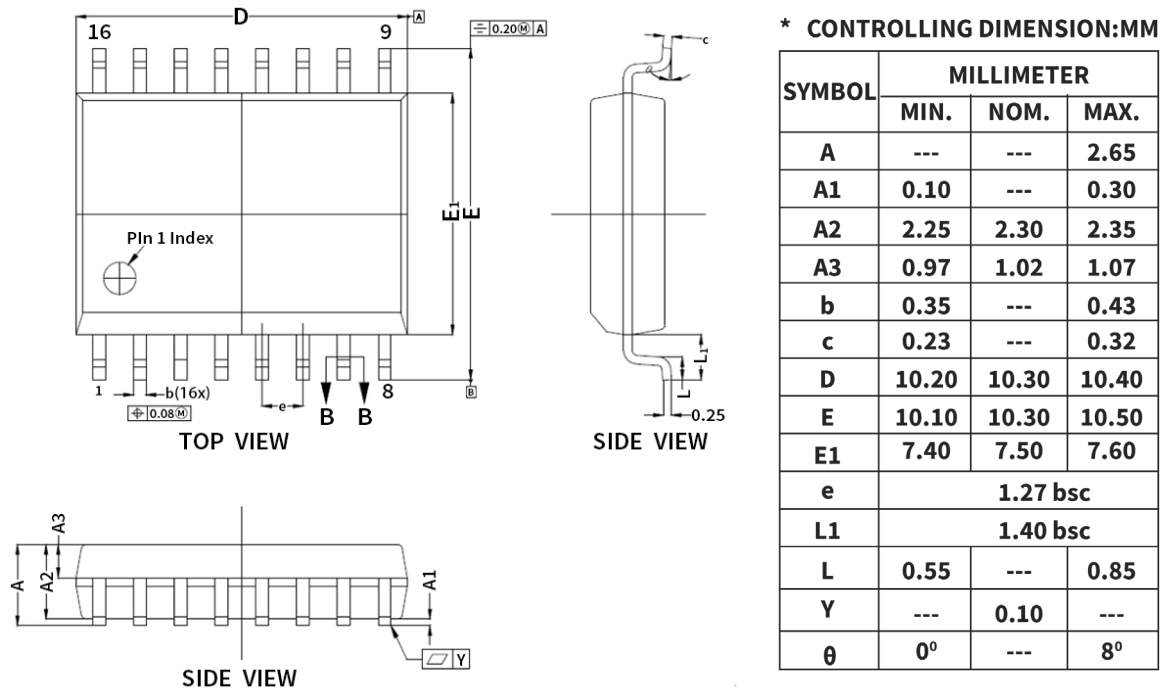


Figure 9.1 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

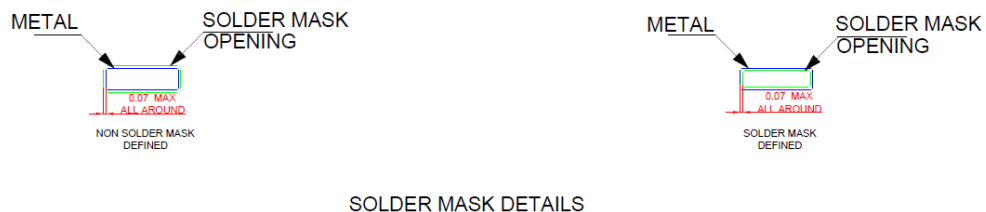
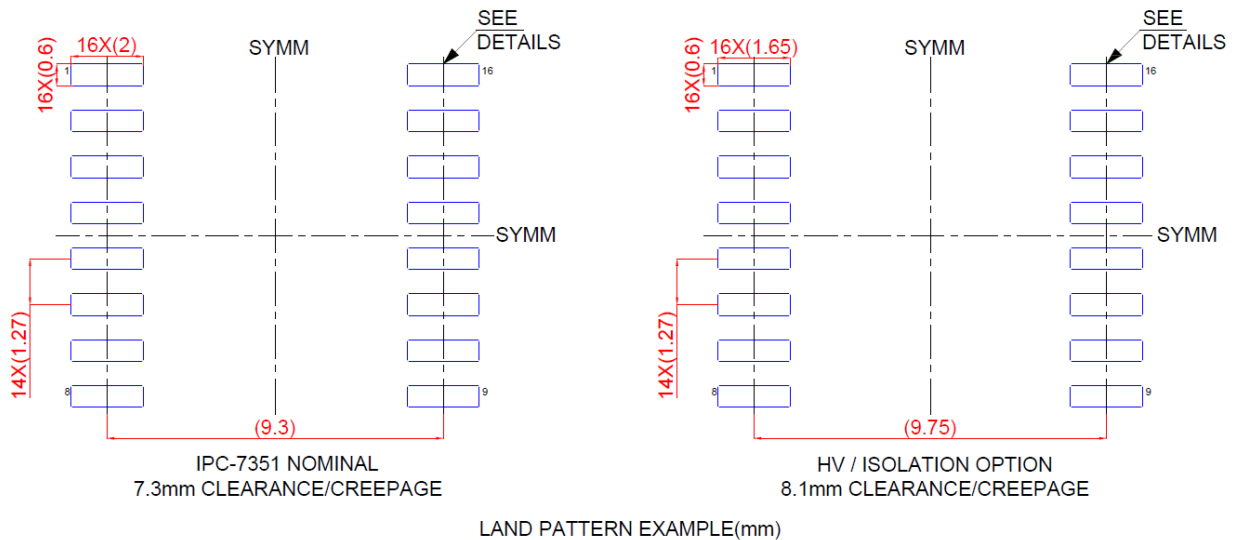
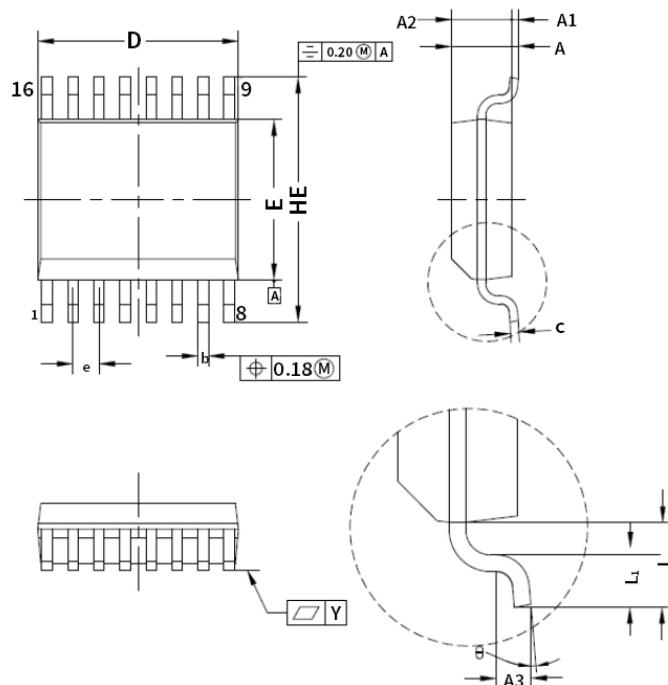


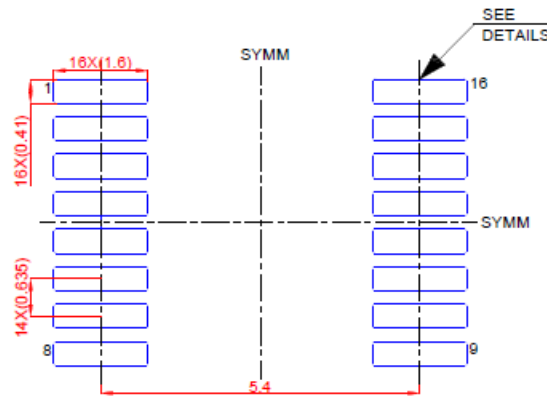
Figure 9.2 SOP16(300mil)/SOW16 Package Board Layout Example



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.73	---	---	0.068
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.20	---	0.31	0.008	---	0.012
c	0.18	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E	3.80	---	4.00	0.150	---	0.157
HE	5.80	---	6.20	0.228	---	0.244
e	0.635 bsc			0.025 bsc		
L	1.00 bsc			0.039 bsc		
L1	0.41	---	0.89	0.016	---	0.035
Y	---	0.09	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
θ	0°	---	8°	0°	---	8°

Figure 9.3 SSOP16 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)

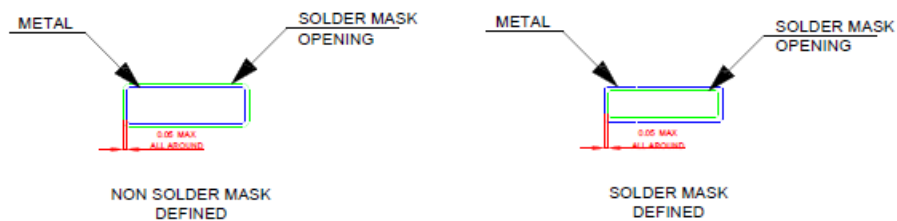


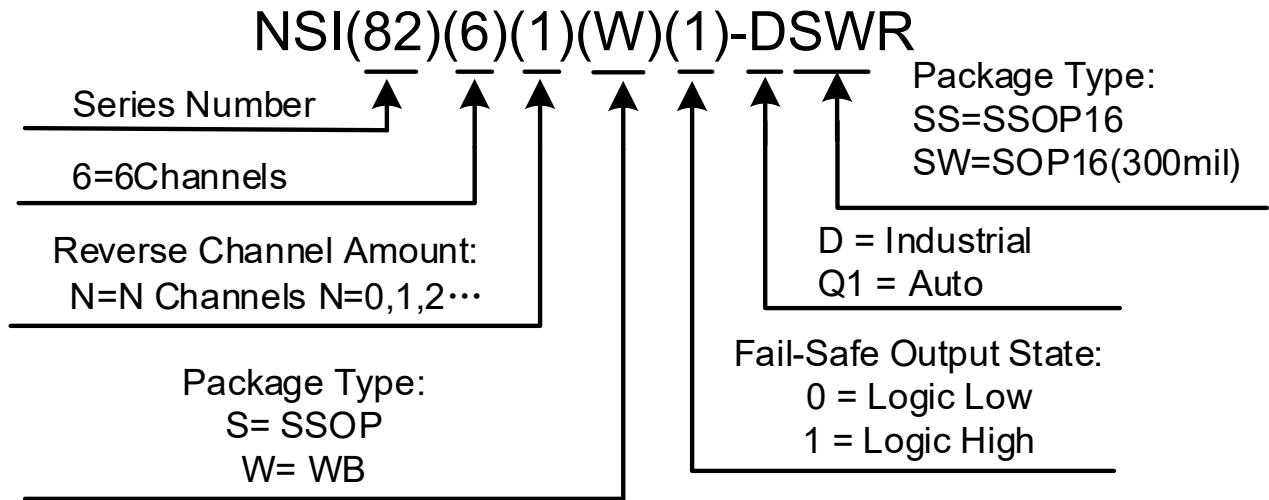
Figure 9.4 SSOP16 Package Board Layout Example

10. Order Information

Part Number	Isolation Rating (kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI8260W0-DSWR	5	6	0	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8260W1-DSWR	5	6	0	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8261W0-DSWR	5	5	1	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8261W1-DSWR	5	5	1	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8262W0-DSWR	5	4	2	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8262W1-DSWR	5	4	2	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8263W0-DSWR	5	3	3	150	Low	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8263W1-DSWR	5	3	3	150	High	-55 to 125°C	2	SOP16 (300mil)	SOW16	1000
NSI8260S0-DSSR	3	6	0	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSI8260S1-DSSR	3	6	0	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500
NSI8261S0-DSSR	3	5	1	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSI8261S1-DSSR	3	5	1	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500
NSI8262S0-DSSR	3	4	2	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSI8262S1-DSSR	3	4	2	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500
NSI8263S0-DSSR	3	3	3	150	Low	-55 to 125°C	1	SSOP16	SSOP16	2500
NSI8263S1-DSSR	3	3	3	150	High	-55 to 125°C	1	SSOP16	SSOP16	2500

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

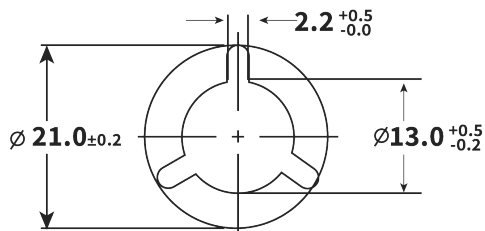
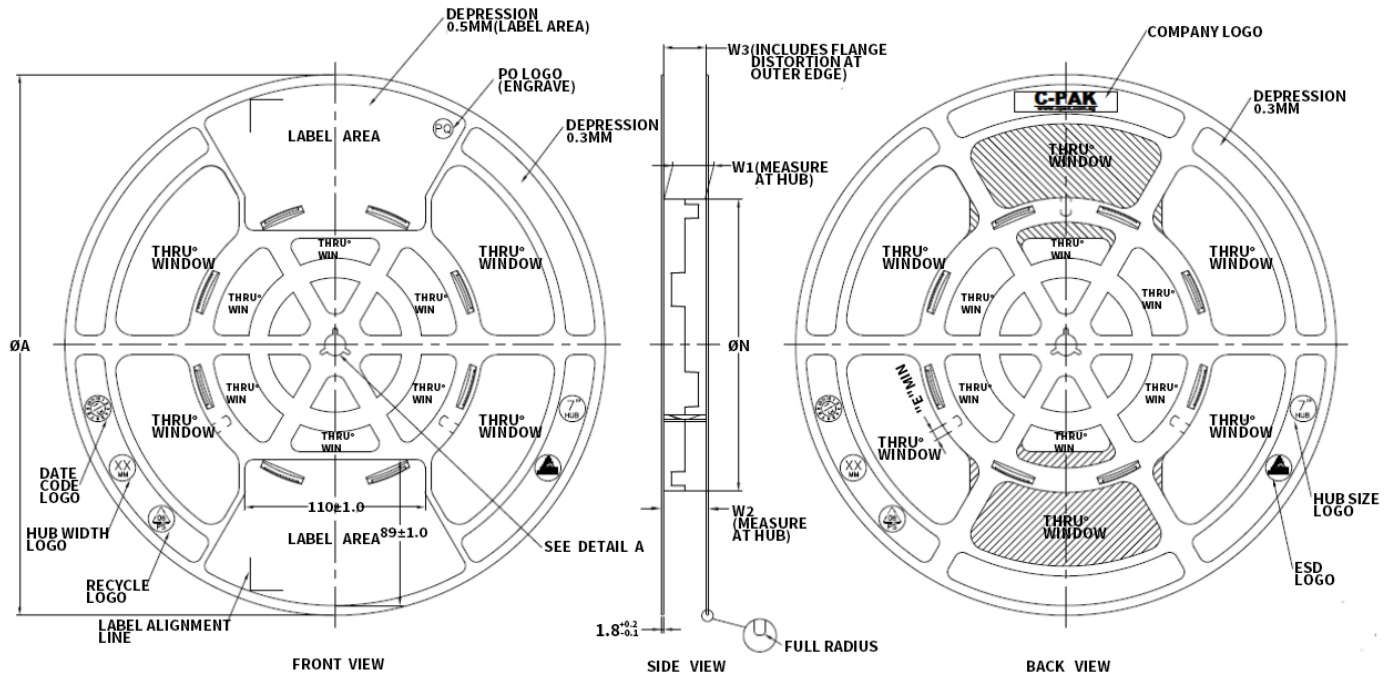
Part Number Rule:



11. Documentation Support

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolator selection guide</i>
NSI826x	tbd	tbd	tbd	tbd

12. Tape and Reel Information

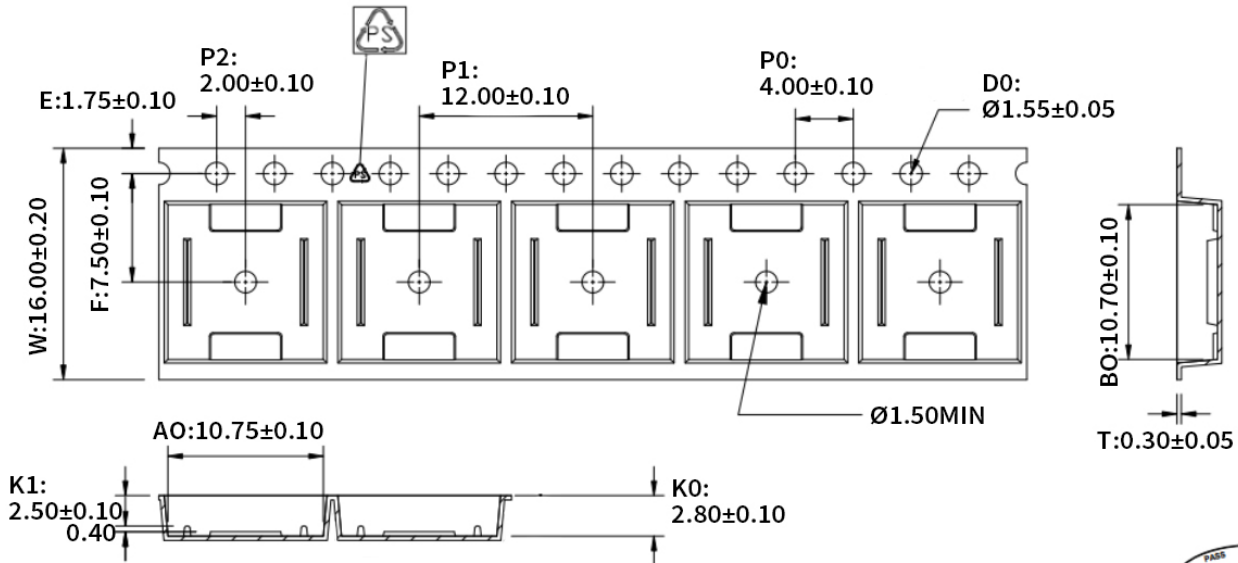


**ARBOR HOLE
DETAIL A
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	$\varnothing A$ ± 2.0	$\varnothing N$ ± 2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^6 TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^5 & BELOW 10^5	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^9 TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Reel Information (for all packages)



1. 1.10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity: $10^5 \sim 10^{10} \Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

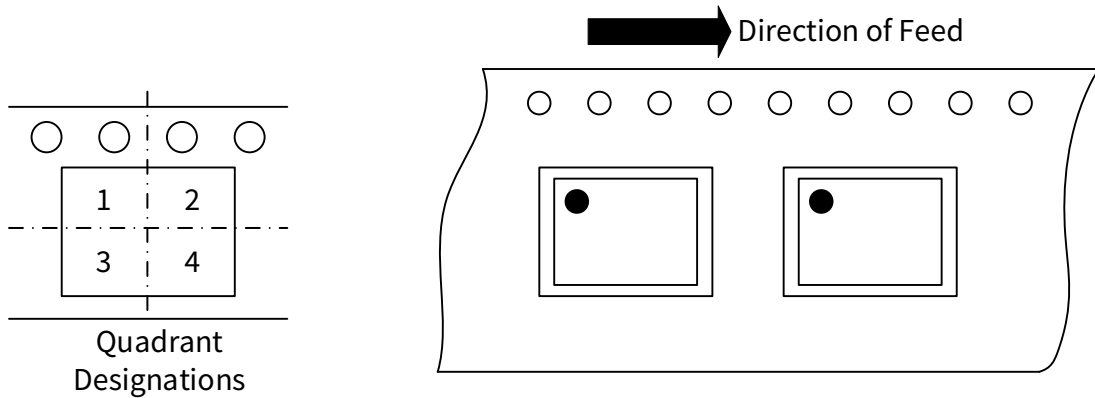


Figure 12.2 Tape Information of SOP16(300mil)

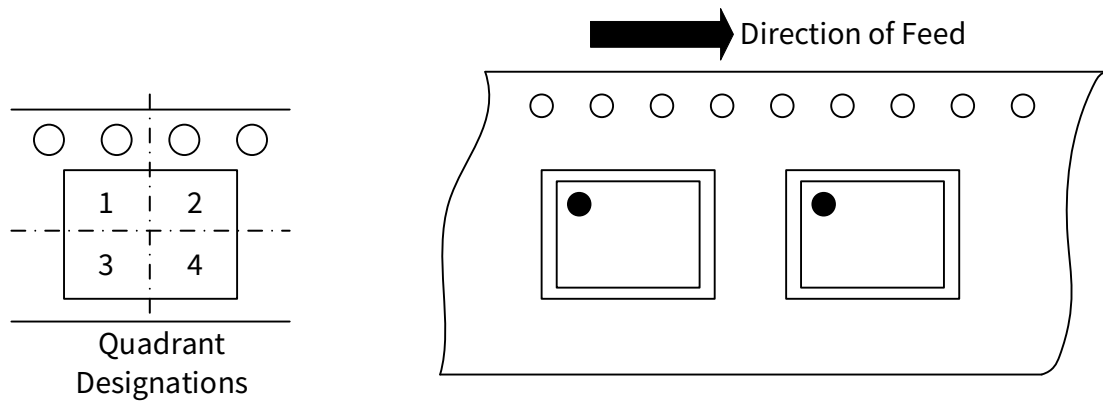
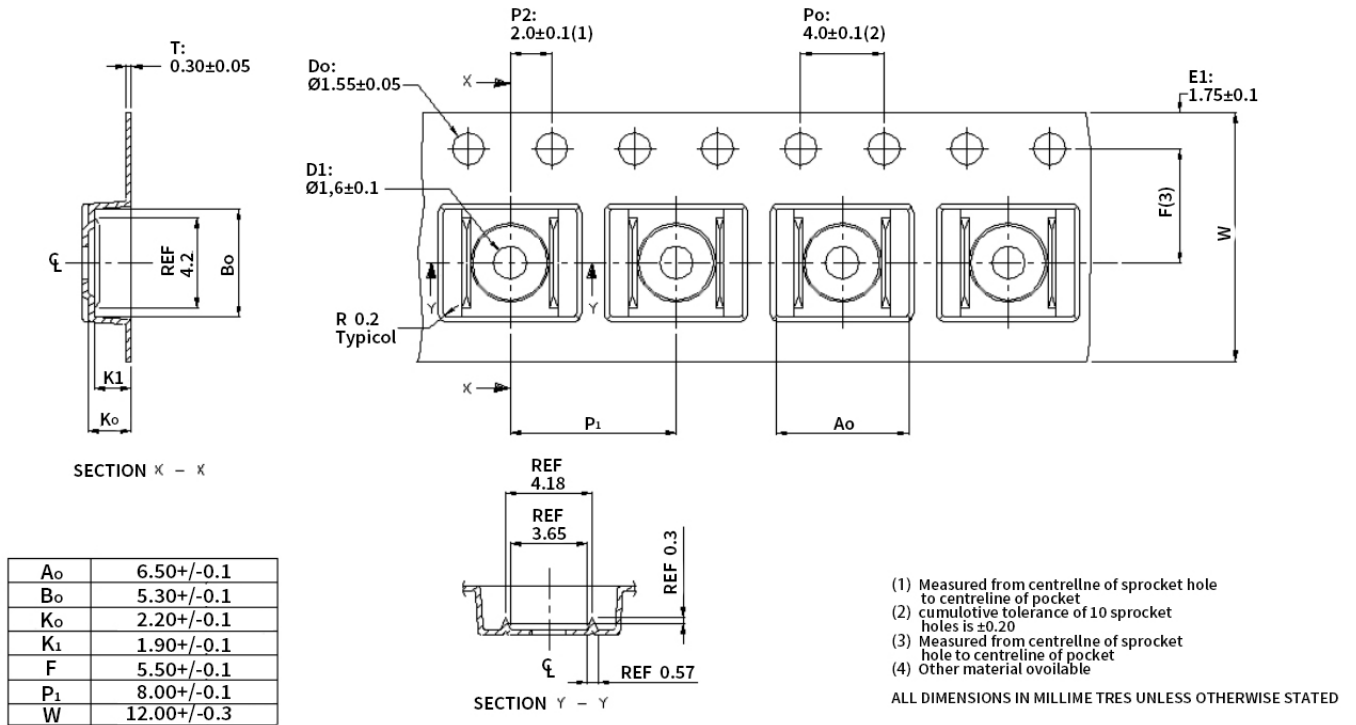


Figure 12.3 Tape Information of SSOP16

13. Revision history

Revision	Description	Date
1.0	Initial version	2020/11/13
1.1	Changed tape and reel information	2020/12/20
1.2	Updated Safety Regulatory	2021/6/28
1.3	Updated Safety-Limiting Values. Update SSOP16 Package Shape and Dimension in millimeters. Changed AEC-Q100 description.	2022/4/25
1.4	Update SOW16\SSOP16 Package Board Layout Example	2022/6/6
1.5	Update SSOP16 CTI and VDE file.	2023/1/12
1.6	Update SOP16 Package, Typical Supply Current Equations	2023/3/22
1.7	Remove SOP16 Package. Update Safety certification info throughout the document. Correct formatting and images.	2024/4/3
1.8	Correct formatting and images. Update Input characteristics. Update Safety certification info throughout the document. Update Function Description. Update eye diagram.	2025/1/13

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Suzhou Novosense Microelectronics Co., Ltd